

MS-7B00 Ver:1.1

CPU:
AMD AM4

System Chipset:
Promontory B350
(Performance gaming)

Main Memory:
DDR IV * 4 MAX:64 GB

VRM
RT8894A 4+2

On Board Chipset:
LPC Super I/O --NCT6795D
LAN I211AT
Azalia CODEC - Realtek ALC1220
ASM2142 USB3.1 Gen2
ASM1061 (B350 on ly)

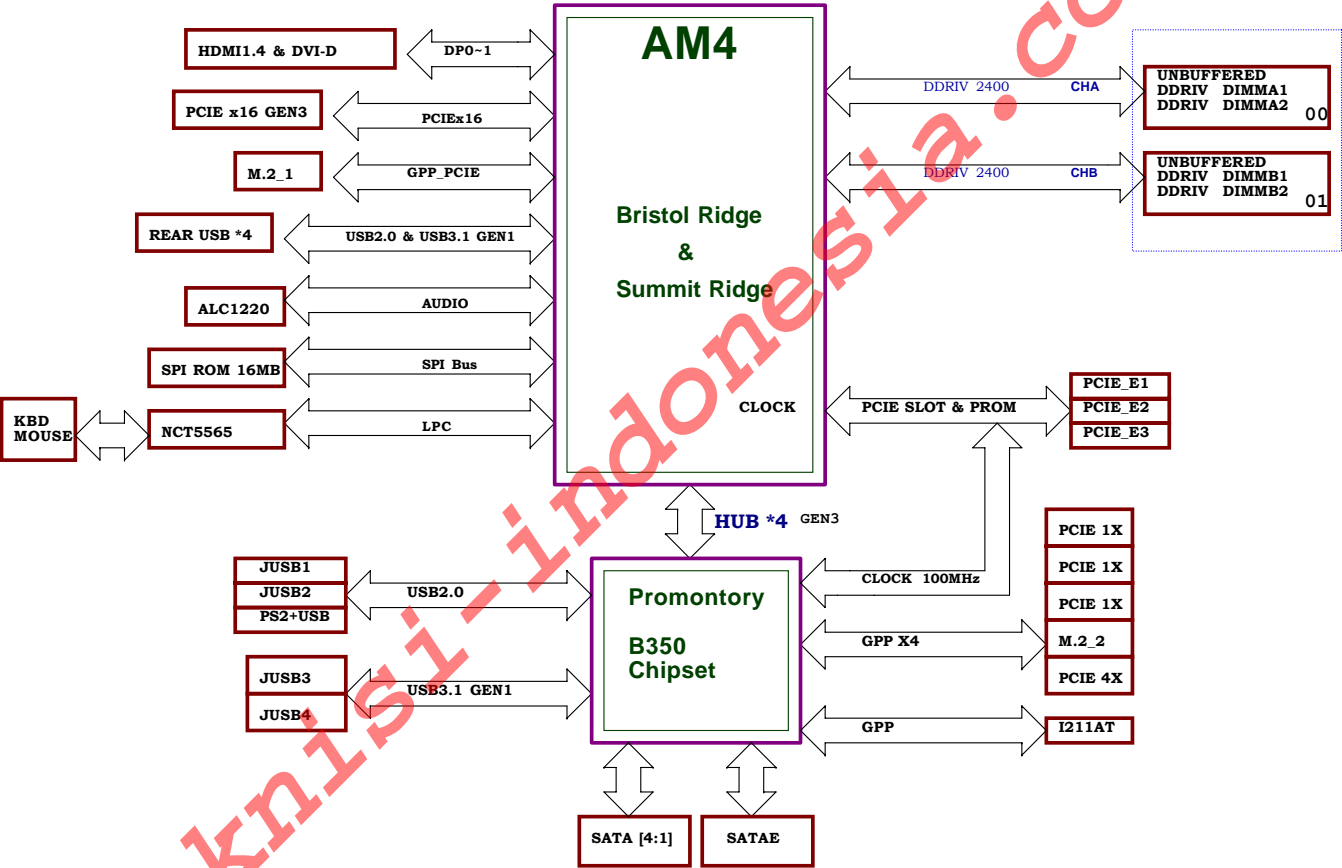
Expansion Slots:

From CPU
PCI Express X16 Slot * 1
PCI Express X8 Slot * 1

From FCH
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
PCI Express X4 Slot * 1

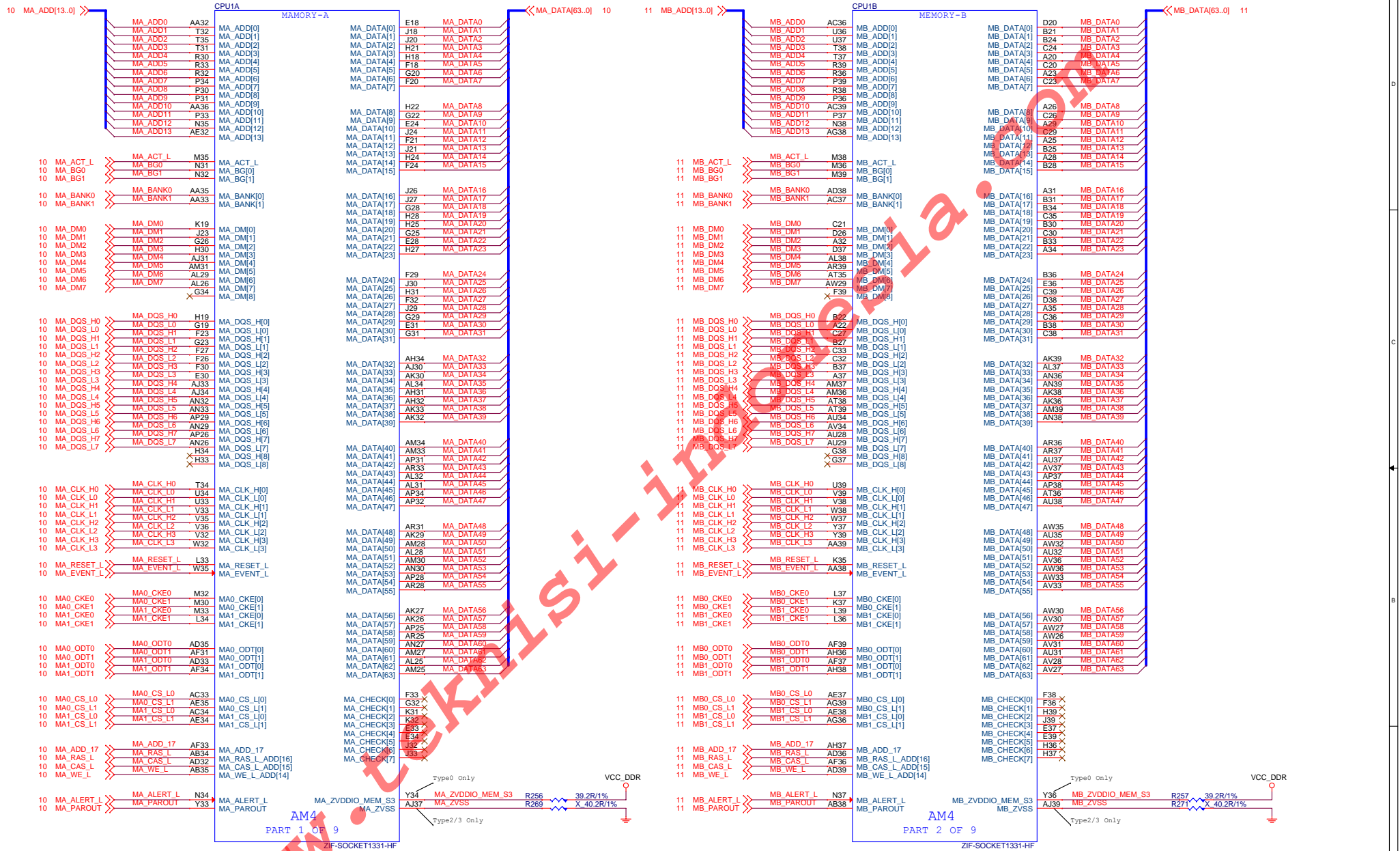
OCF IC:
UP6273

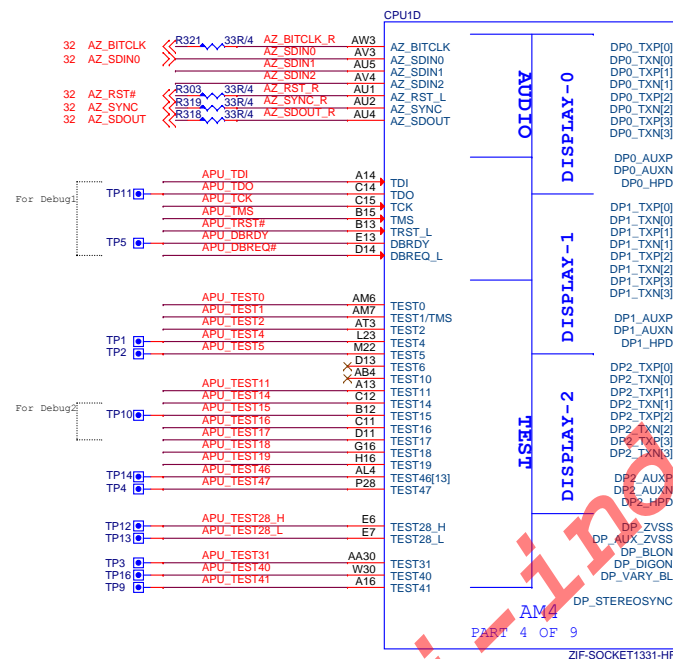
FUSION BLOCK DIAGRAM



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23 / 24 Audio ALC887	
25 USB Rear PS2+USB2.0	
26 USB Rear LAN+USB3.1 GEN1	
27 USB Front Side	
28 SATA Connector	
29 DVI Connector	
30 DP to VGA ITE6516	
31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTM-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	

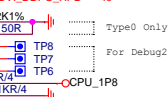




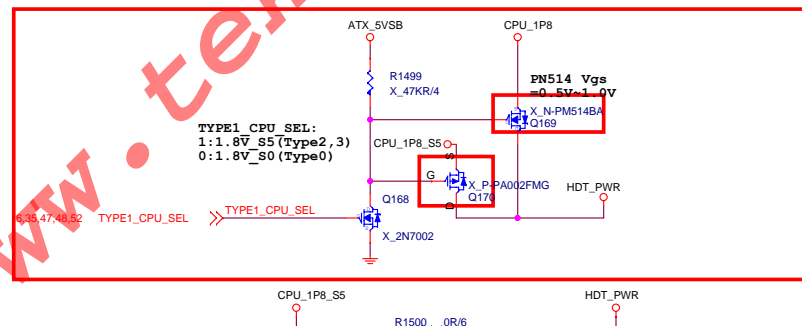


For HDMI

For DVI

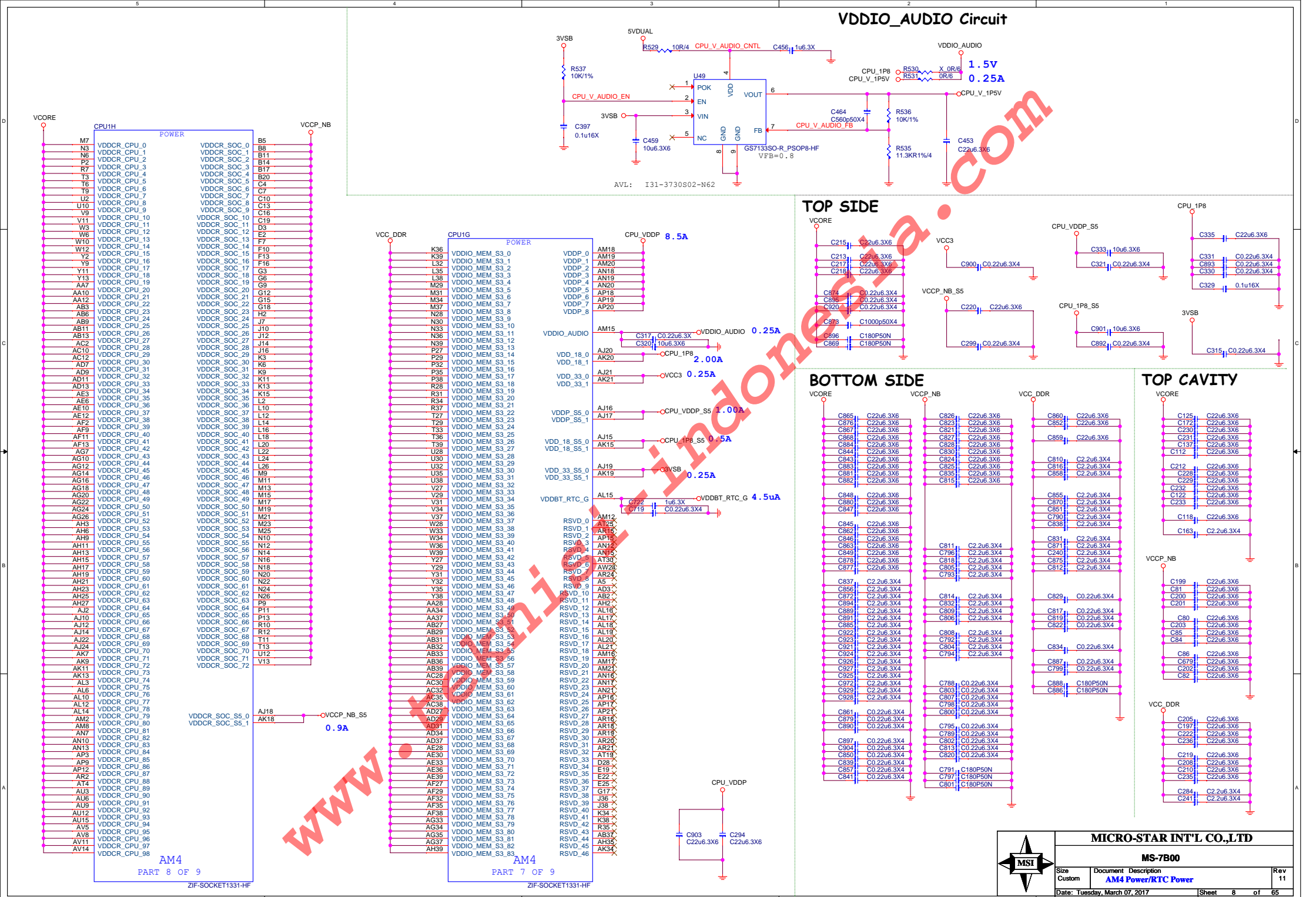


Not support Type2

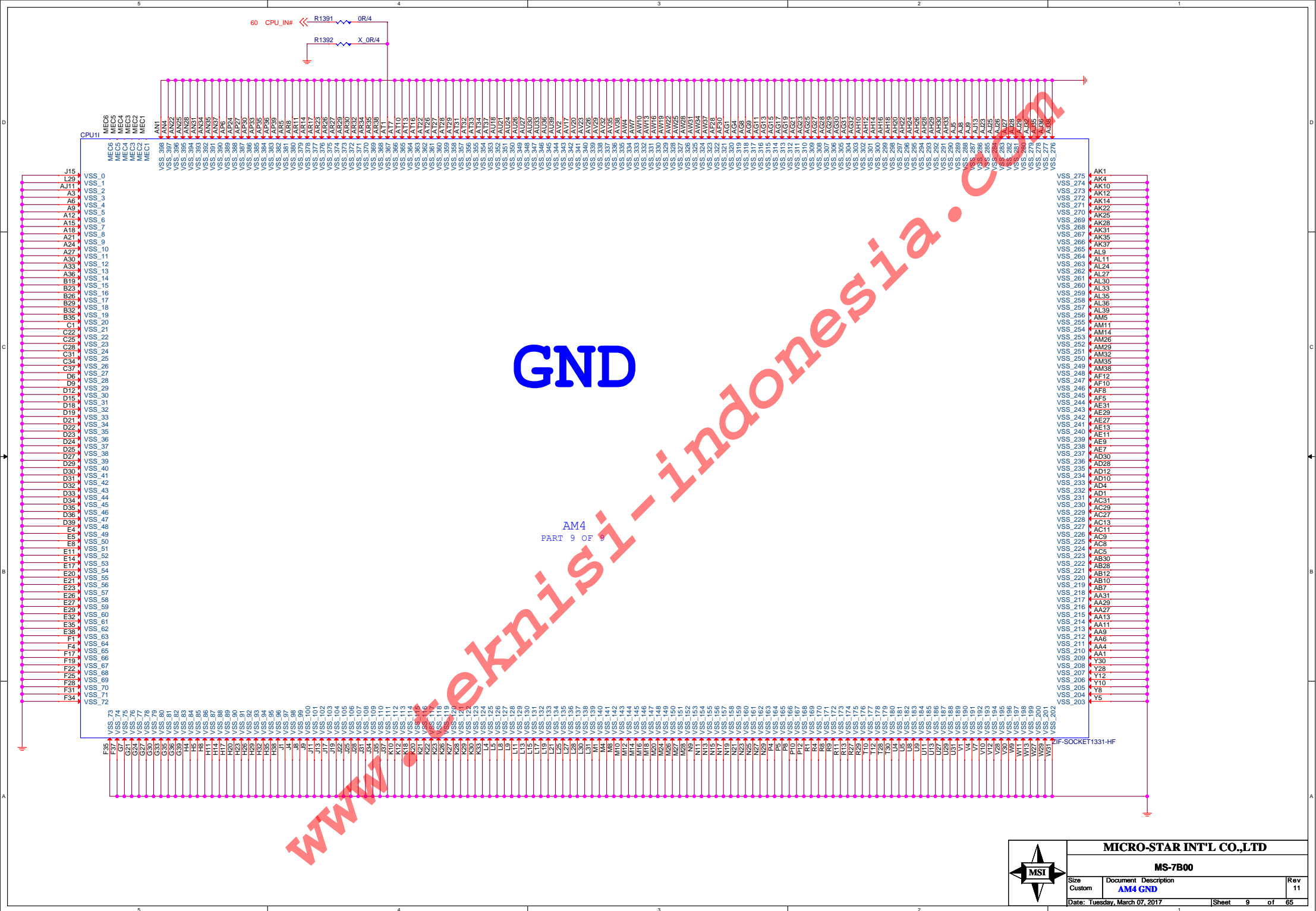


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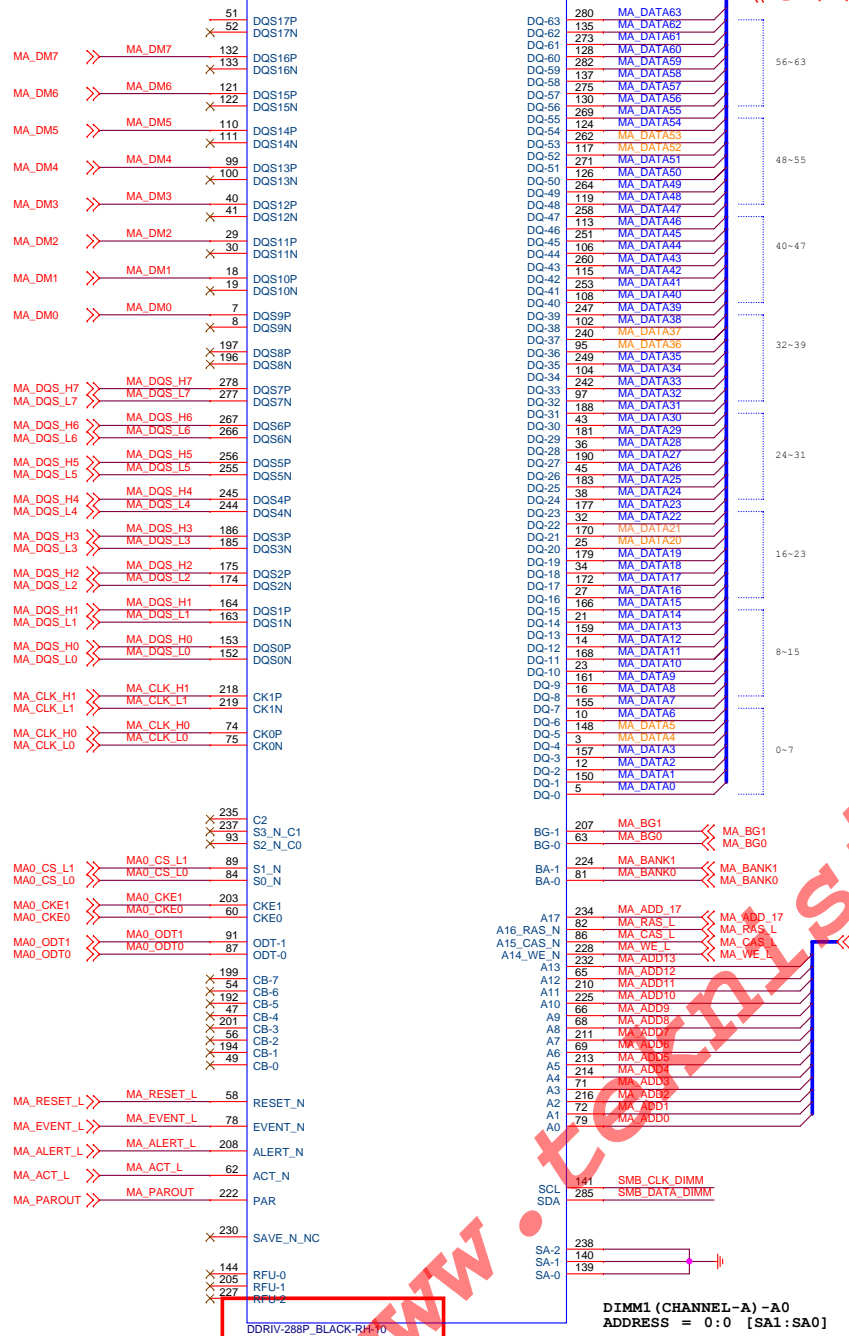
**MS-7B00**

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A1

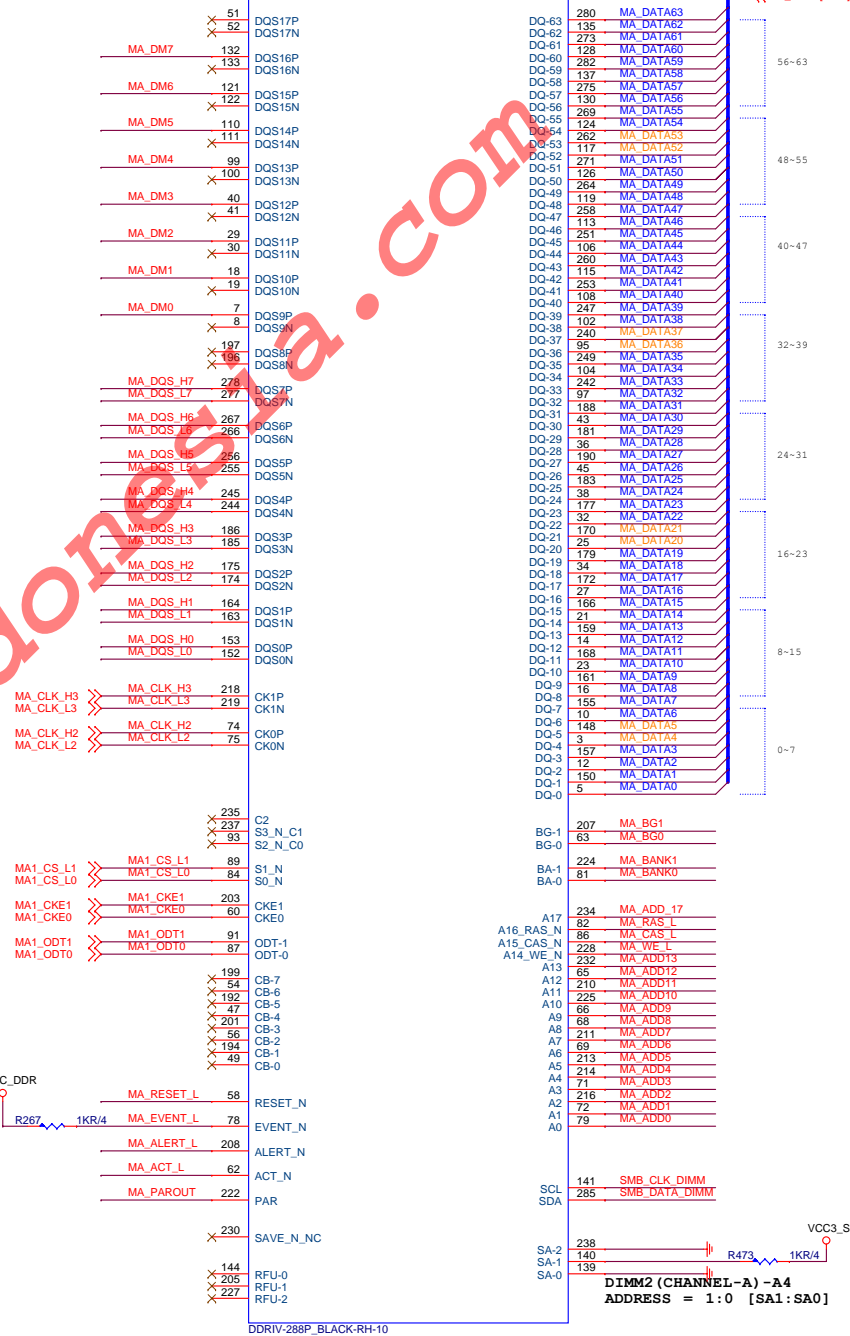
DIMMA1A



SCLK0 SCLK0 R427 OR/4 SMB_CLK_DIMM
SDATA0 SDATA0 R431 OR/4 SMB_DATA_DIMM

<< MA_DATA[63..0]

DIMMA2A



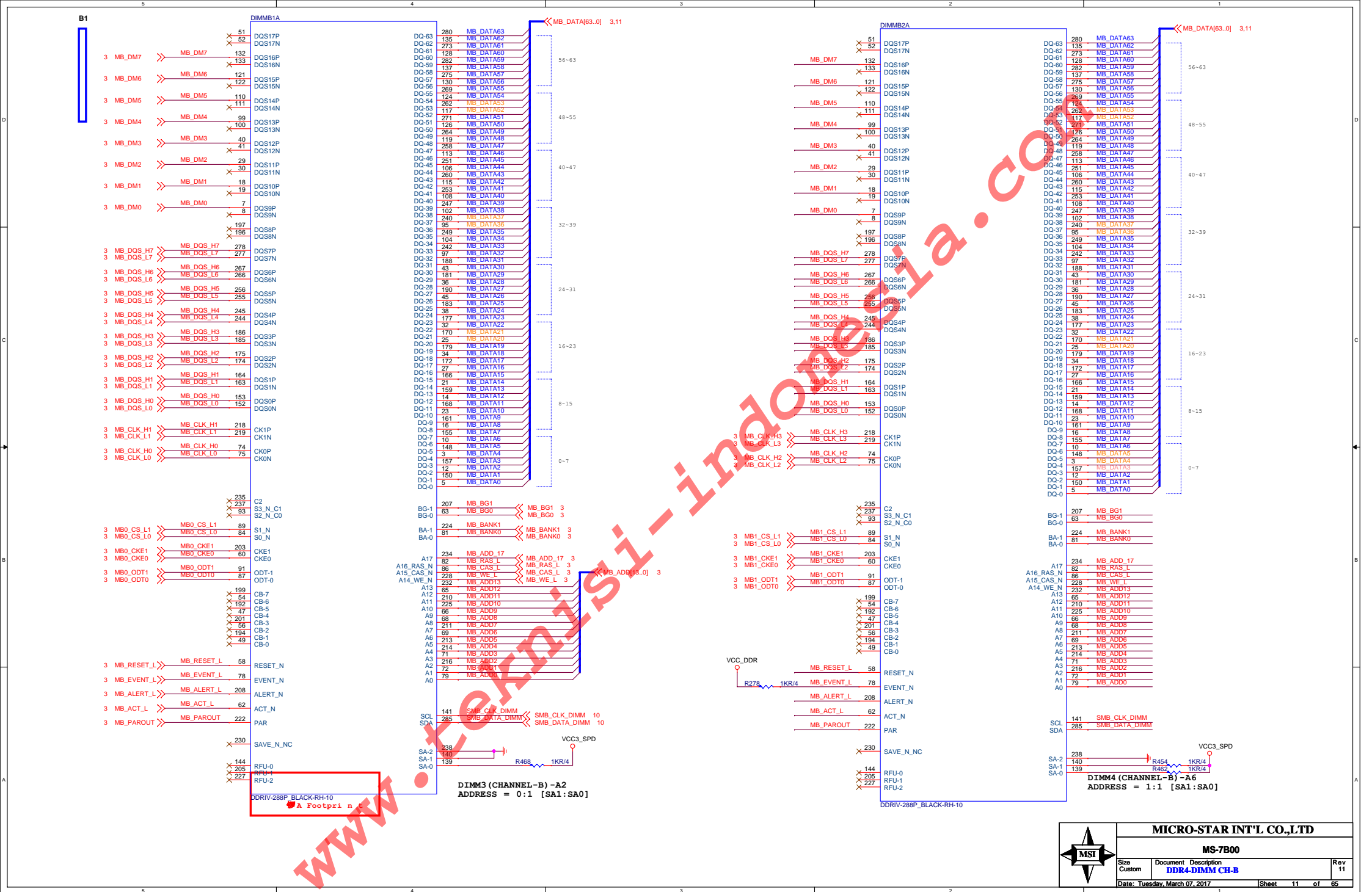
DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]



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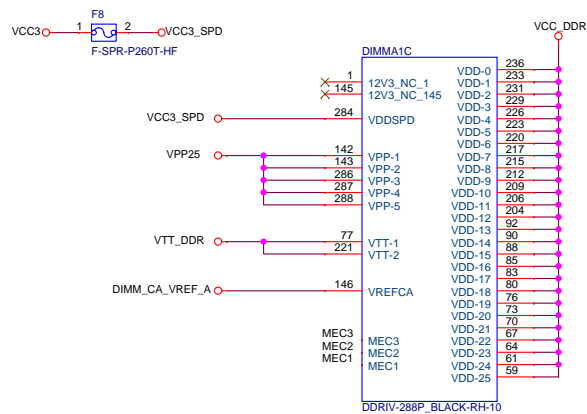
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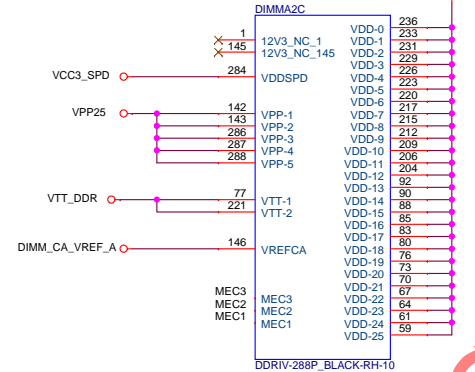
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Custom	DDR4-DIMM CH-B	11
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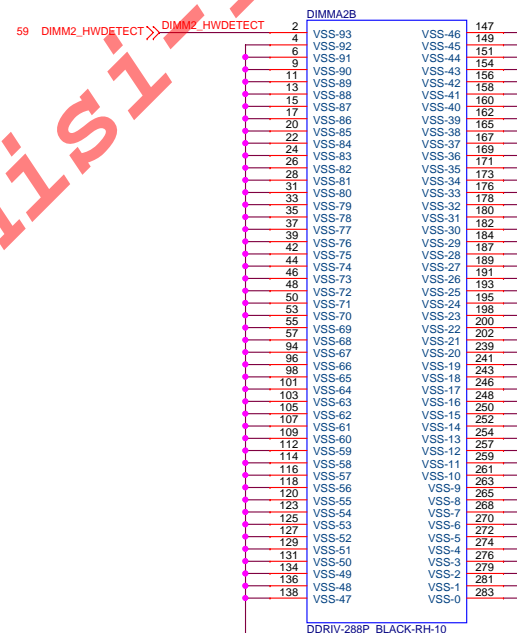
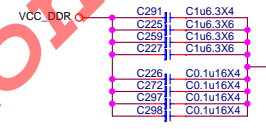
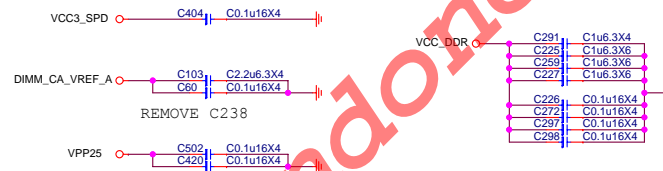
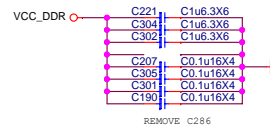
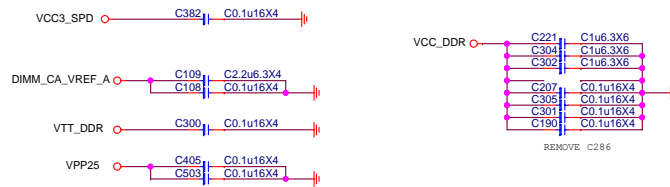
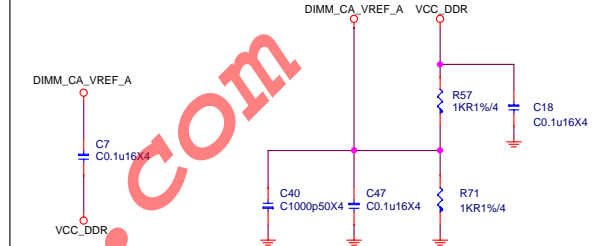


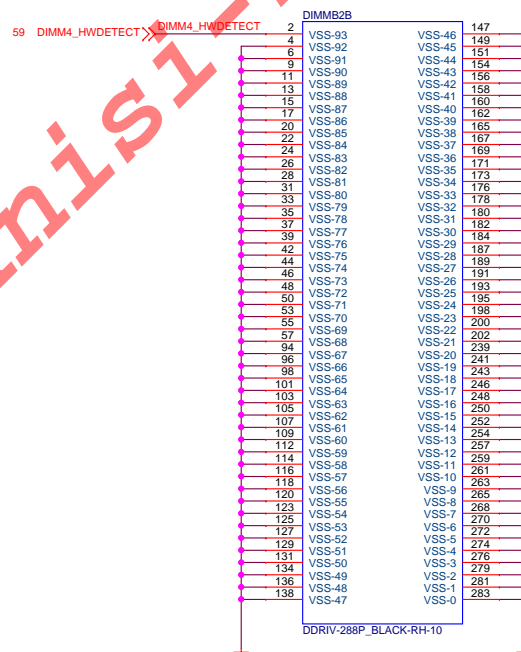
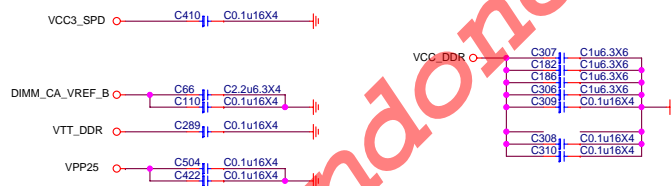
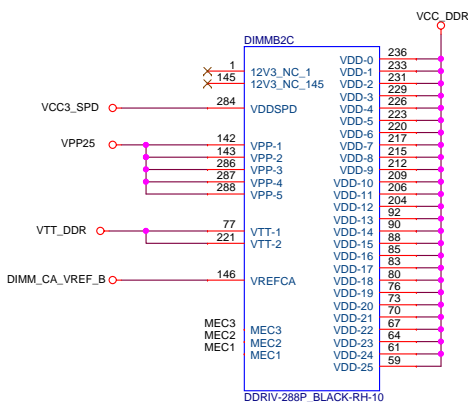
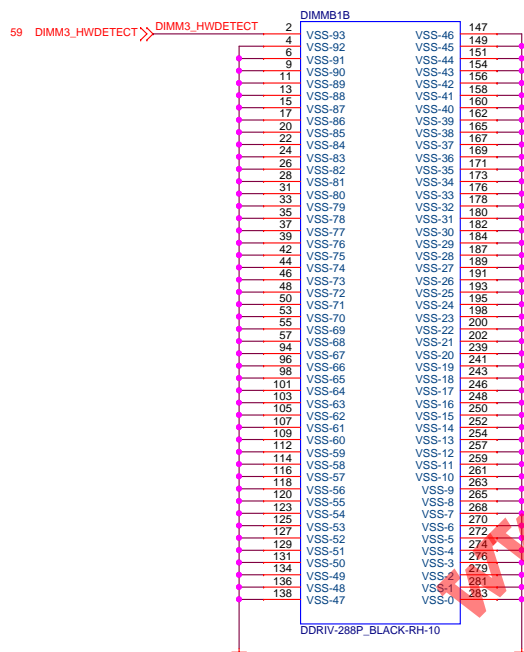
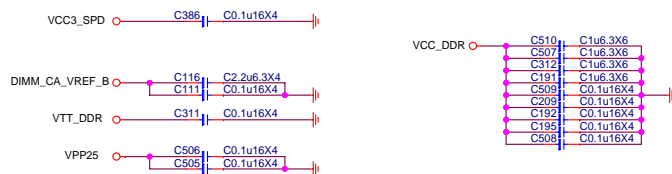
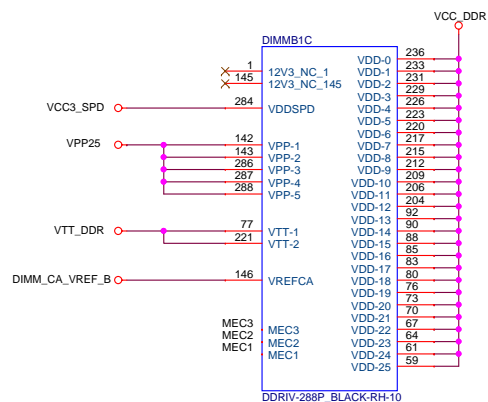
DIMM SLOT PN BY SPEC



DDR VREF

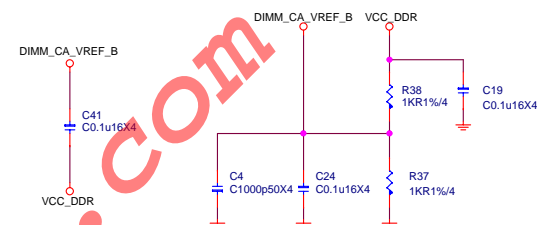
(place resistors close to DIMMs)





DDR VREF

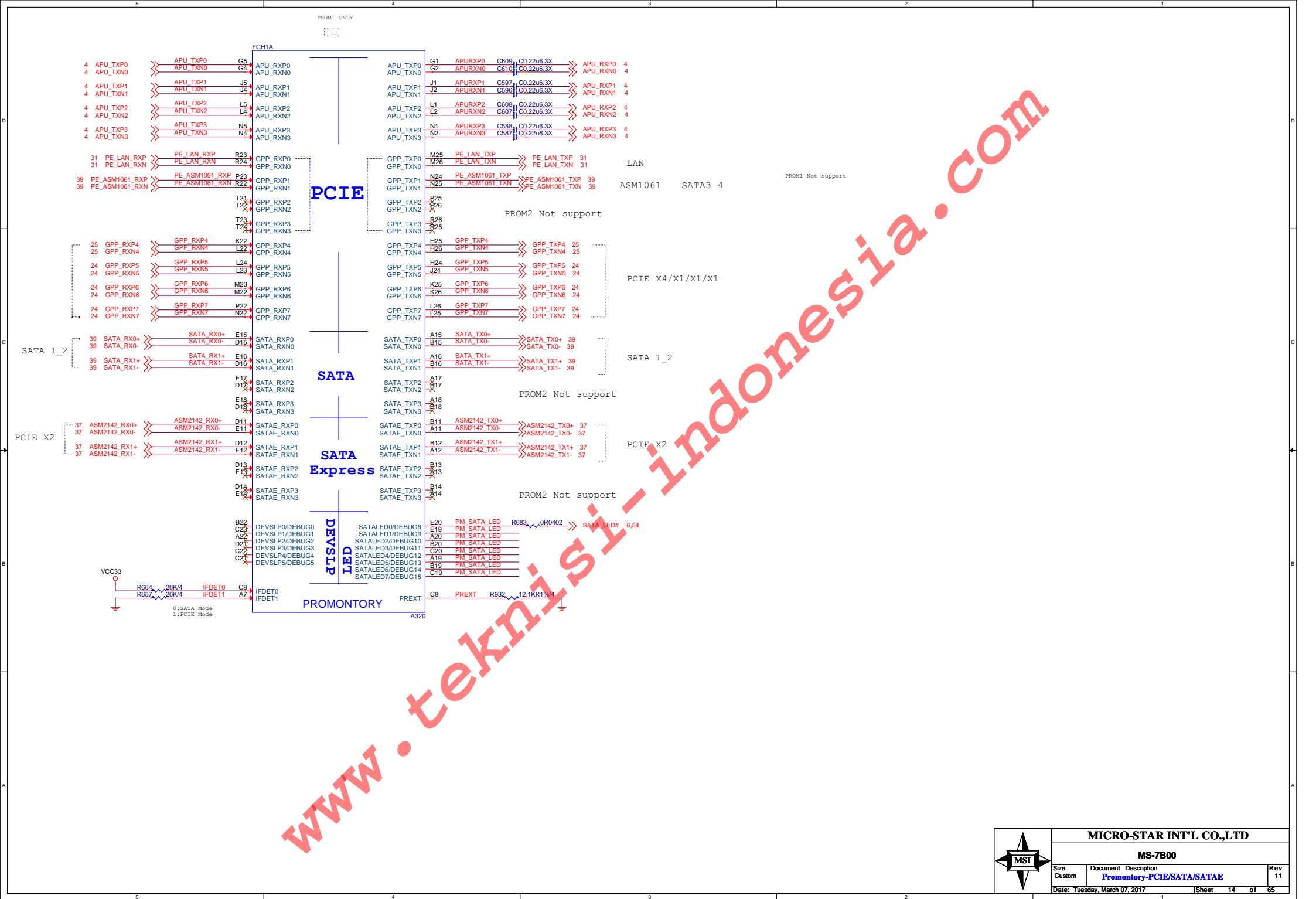
(place resistors close to DIMMs)



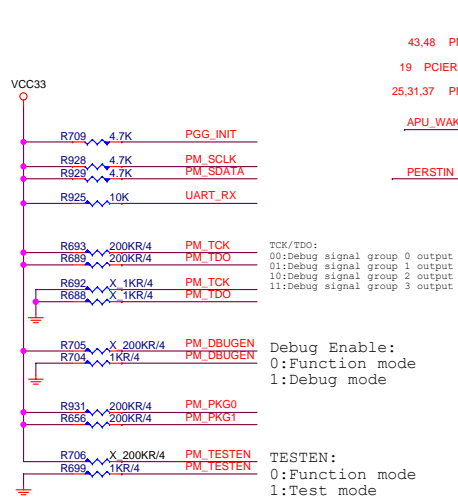
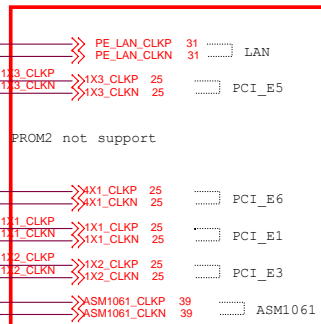
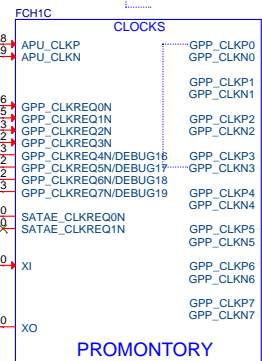
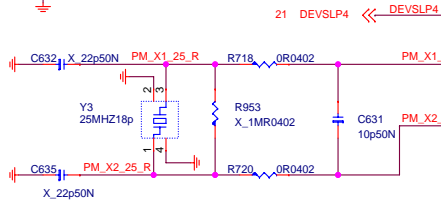
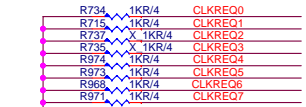
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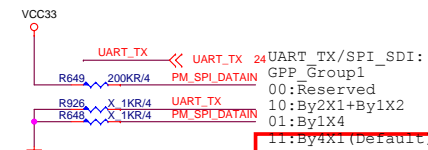
Not implemented: Left unconnected.
Need confirm whether can floating



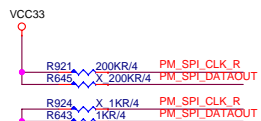
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output

Debug Enable:
0:Function mode
1:Debug mode

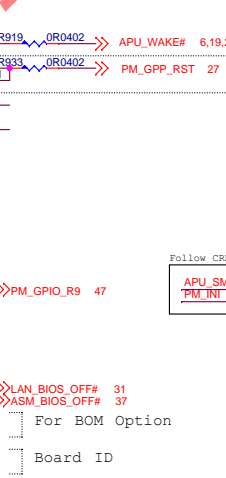
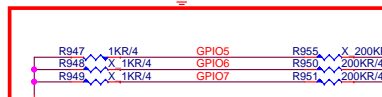
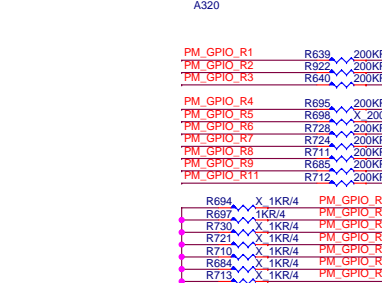
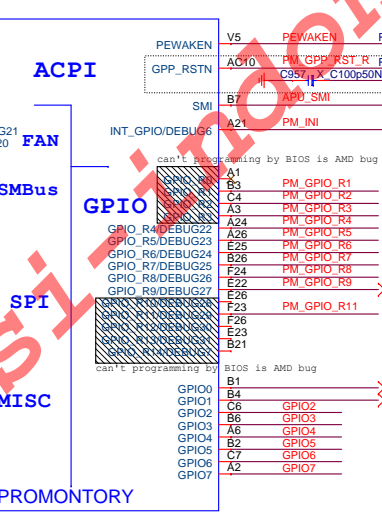
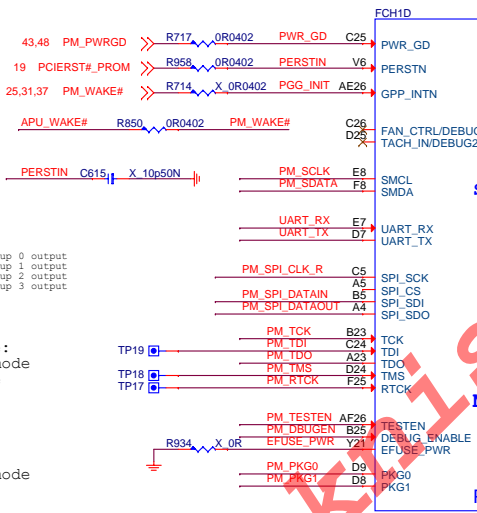
TESTEN:
0:Function mode
1:Test mode



11:By4X1(Default)



SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2



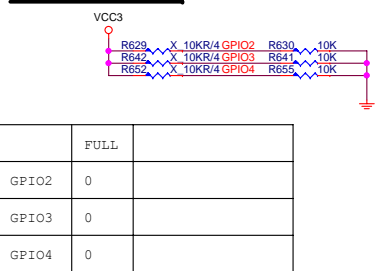
Co-layer GPP_RSTN Reset for meet FCH sequence. See 55553.
PERSTN to GPP_RSTN delay 200us

Follow CRB



LAN BIOS_OFF# R673 200KR/4
ASM BIOS_OFF# R671 200KR/4

BOM OPTION



	FULL	
GPIO2	0	
GPIO3	0	
GPIO4	0	



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GND

PROMONTORY



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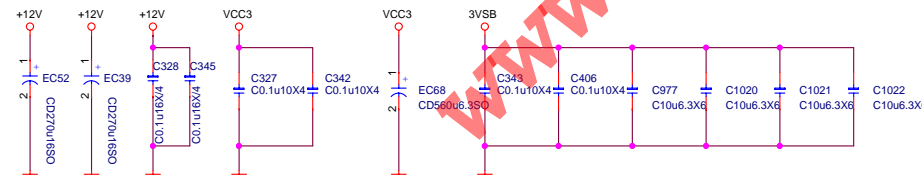
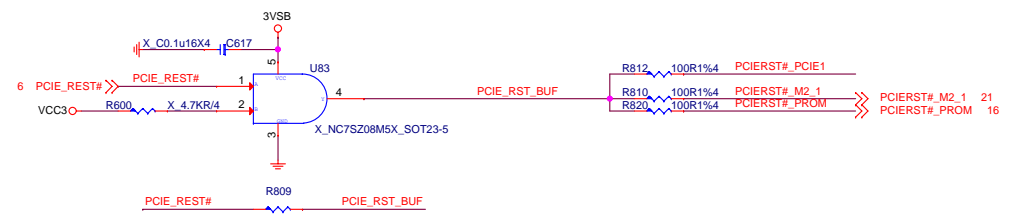
PCI EXPRESS x16 Slot

3.3V
12V

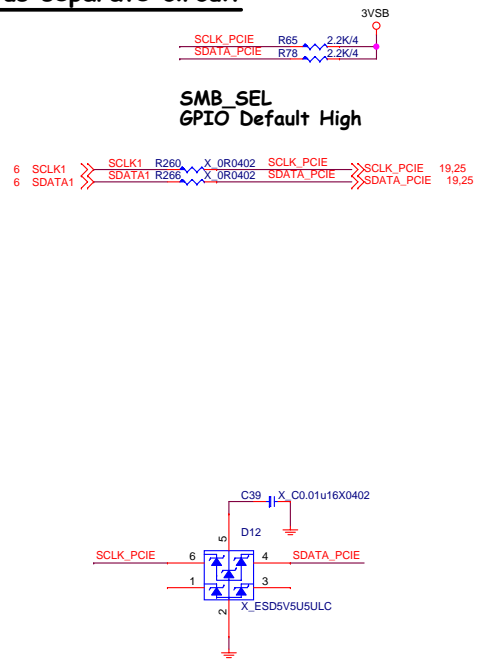
3.0A
5.5A



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SMBus separate circuit



PCI EXPRESS Switch

For PCIE2 & PCIE4



PCIE Lanes control circuit

	PCIE_CNTL	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0



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2016.05.31 Update M.2 PartNumber & Footprint
ON1-7A58001-L06
SLOT_NGFFCARD67_31

SCREW1
SCREW
SCREW

SCREW3
SCREW
SCREW

SHIELD1
SCREW
SHIELD

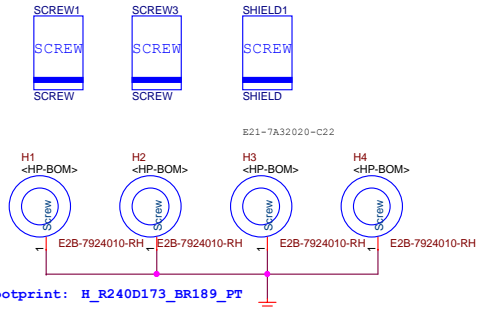
E21-7A32020-C22

H1 <HP-BOM>
H2 <HP-BOM>
H3 <HP-BOM>
H4 <HP-BOM>

E2B-7924010-RH E2B-7924010-RH E2B-7924010-RH E2B-7924010-RH

Footprint: H_R240D173_BR189_PT

MICRO-STAR INT'L C
MS 7B00



Select M2 PCIE or SATA mode

PCIE0

4 APU_GPP_RXN0
4 APU_GPP_RXP0
4 APU_GPP_TXP0
4 APU_GPP_TXN0

M2_SATA_RXN2
M2_SATA_RXP2
M2_SATA_TXP2
M2_SATA_TXN2

37
36
33
32

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M2_SATA_TXN2
M2_SATA_TXP2
M2_SATA_RXP2
M2_SATA_RXN2

28
27
24
23

21 M2_TXN2
21 M2_TXP2
21 M2_RXP2
21 M2_RXN2

12
13
16
17

GND-10
GND-9
GND-8
GND-7
GND-6
GND-5
GND-4
GND-3
GND-2
GND-1

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ASM1480_TQFN42

U53

AOa+
AOa-
BOa+
BOa-
AOB+
AOB-
BOB+
BOB-
COa+
COa-
DOa+
DOa-
COB+
COB-
DOB+
DOB-
GND-10
GND-9
GND-8
GND-7
GND-6
GND-5
GND-4
GND-3
GND-2
GND-1

1
2
5
6
30
10
11
14
15

AI+
AI-
BI+
BI-
SEL
CI+
CI-
DI+
DI-

M2_RXN0
M2_RXP0
M2_TXP0
M2_TXN0
M2_1_DET
APU_GPP_TXN2
APU_GPP_TXP2
APU_GPP_RXP2
APU_GPP_RXN2

21
21
21
21
6,21
21
21
21
21

M.2

M2_1 SW:
0:SATA
1:PCIE

GPP	0	1	2	3
TYPE0	PCIE	PCIE	SATA	SATA
TYPE2	PCIE	PCIE	PCIE	PCIE
	PCIE	PCIE	SATA	SATA

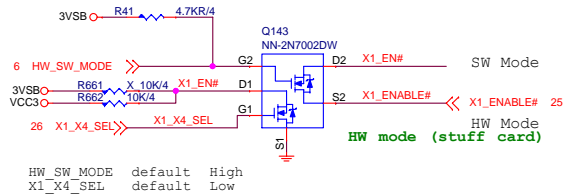
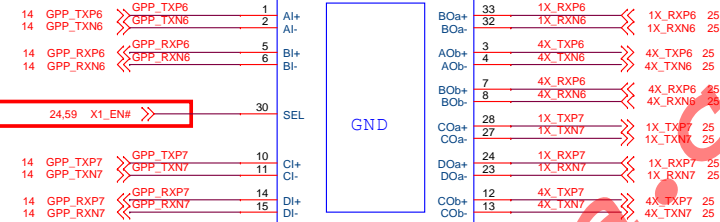
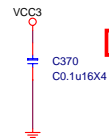
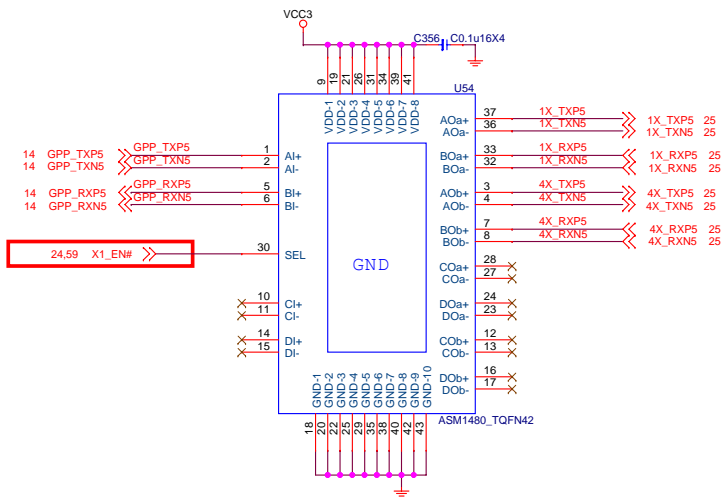
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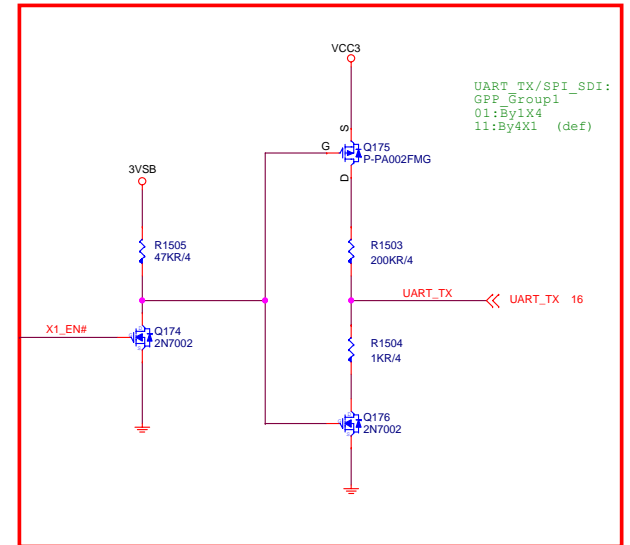
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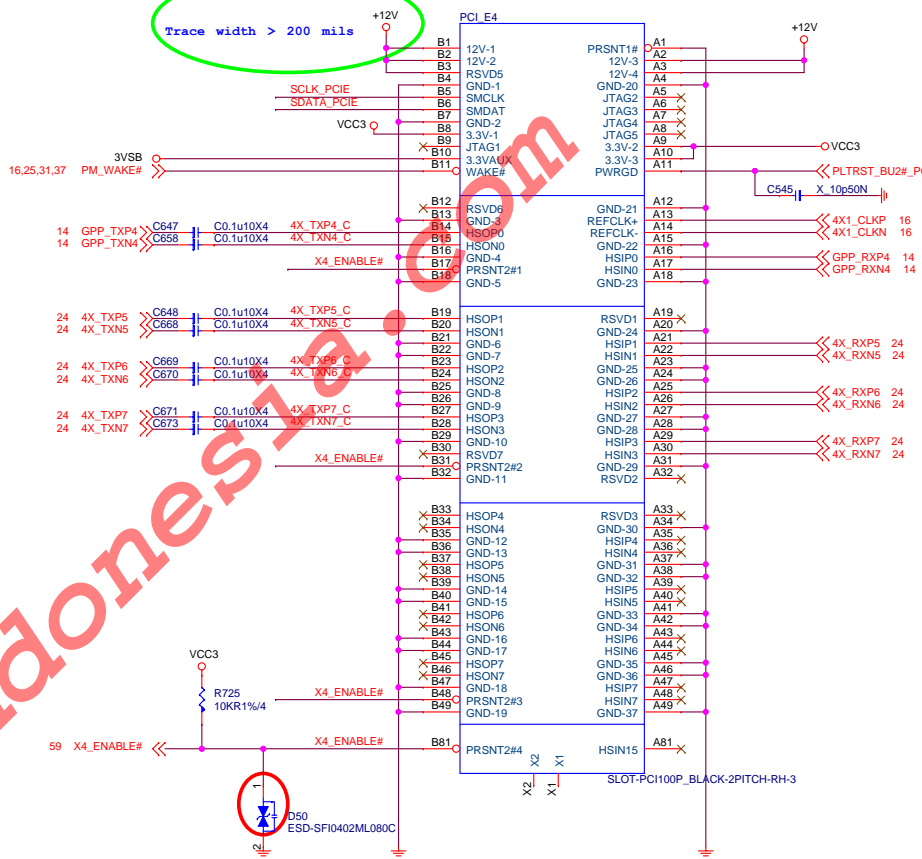
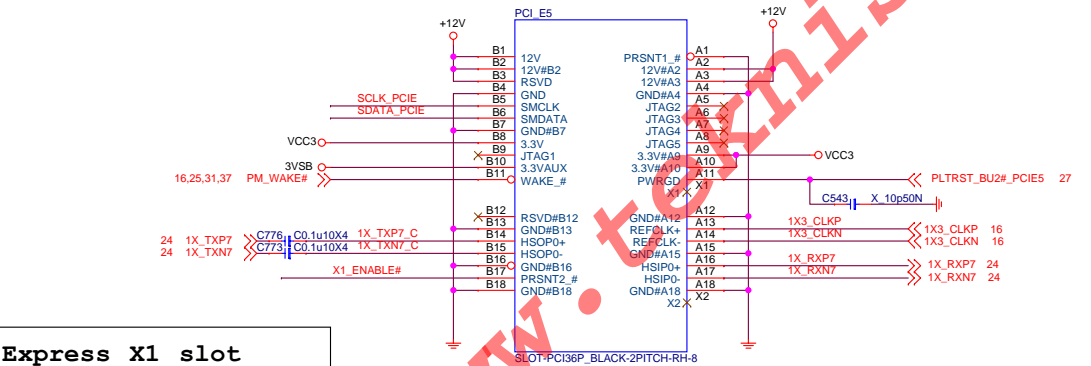
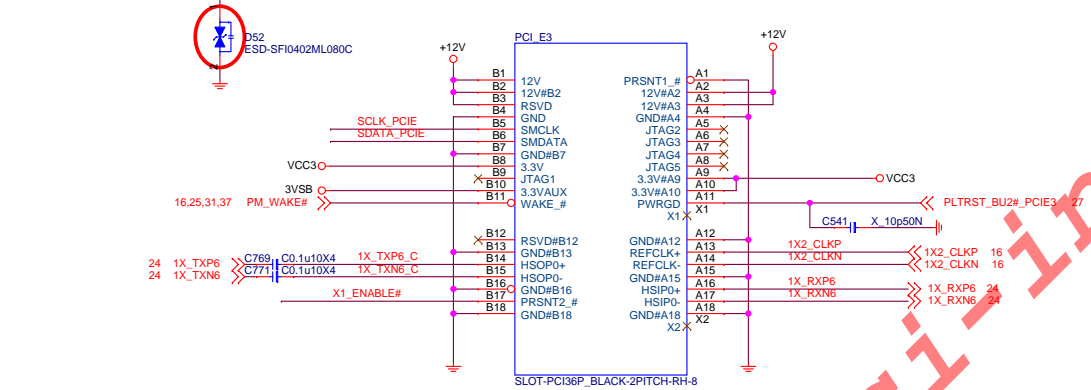
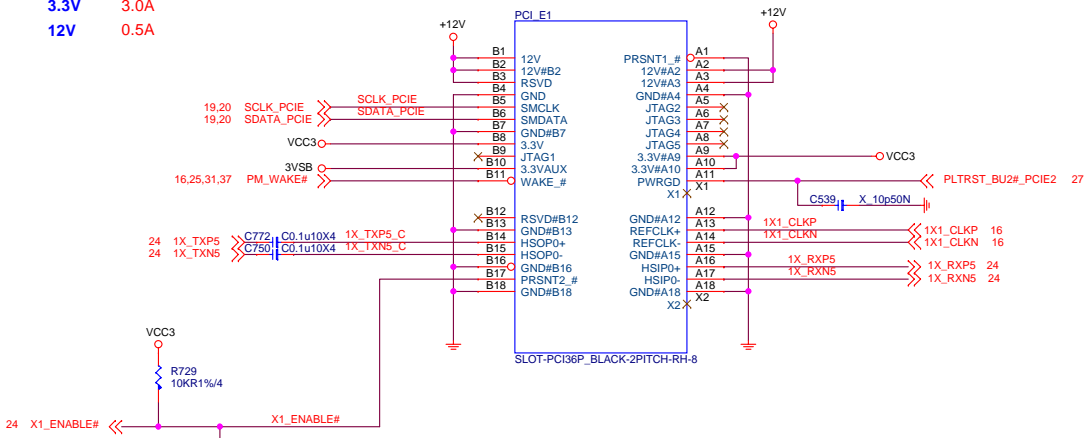


	HW_SW_MODE	X1_X4_SEL	X1_ENABLE#	X1_EN#	UART_TX	
HW MODE	1	0	1	1	H	X4
	1	0	0	0	L	X1
SW MODE	0	1	X	0	L	X1
	0	1	X	1	H	X4




PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V 3.0A
12V 0.5A



PCI Express X1 slot	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

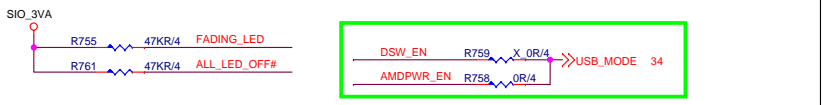
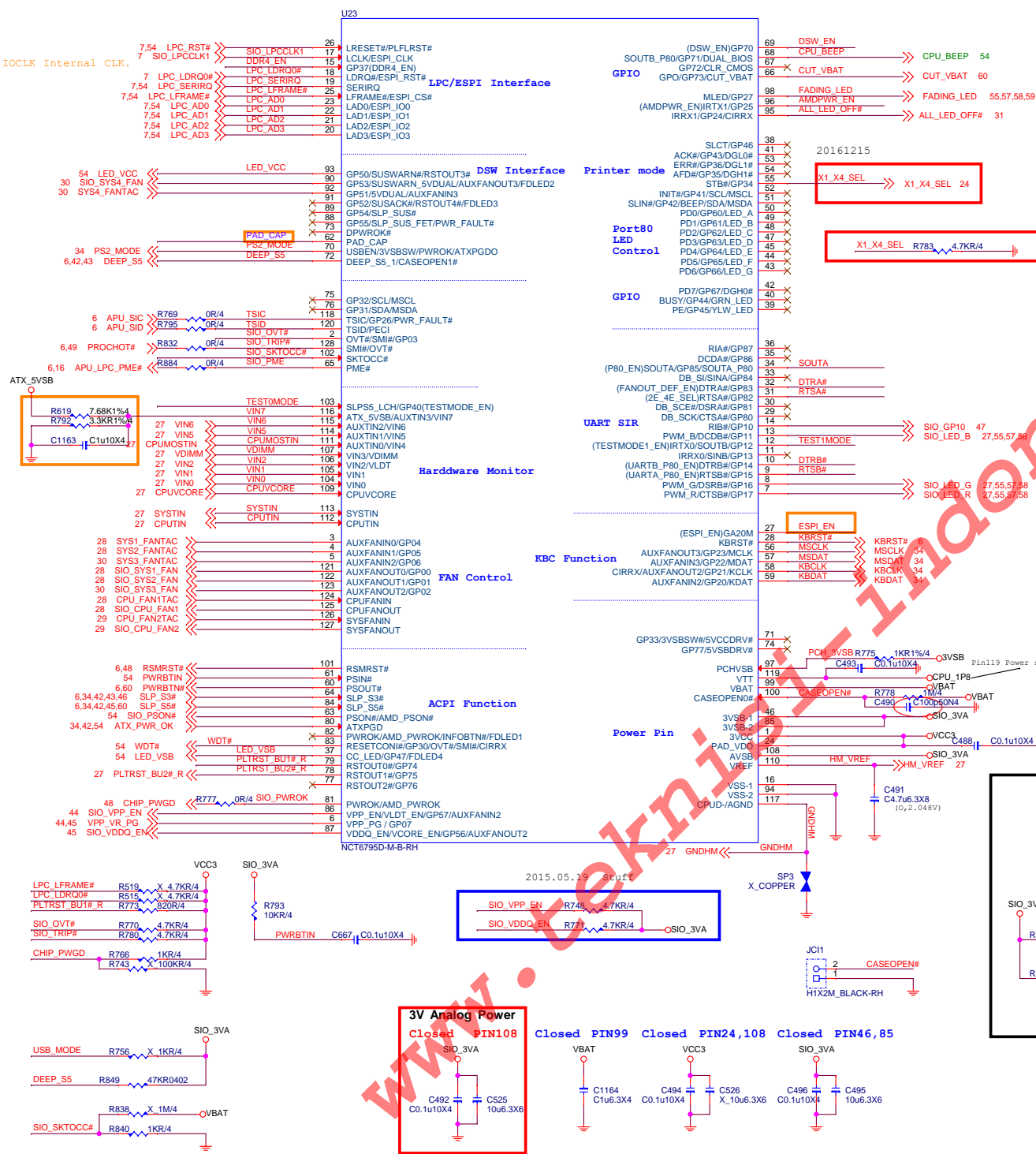


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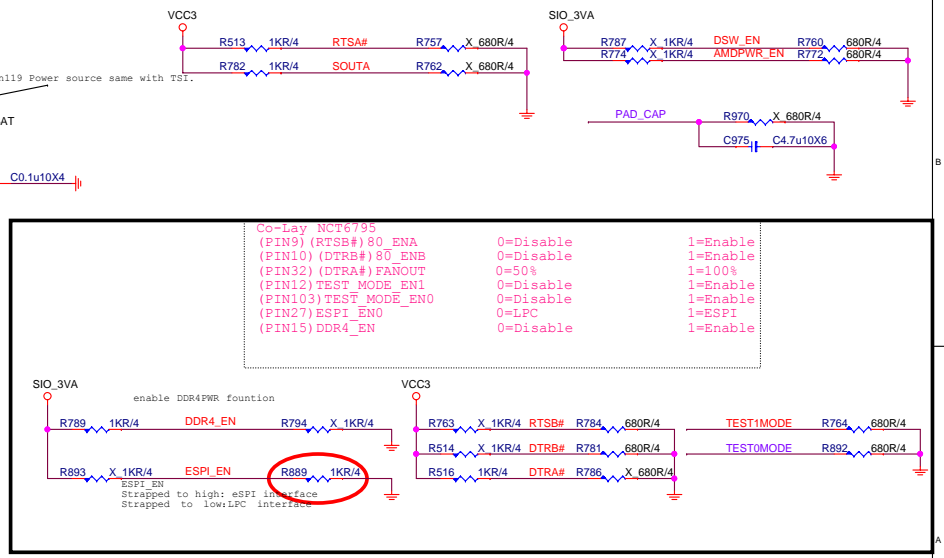
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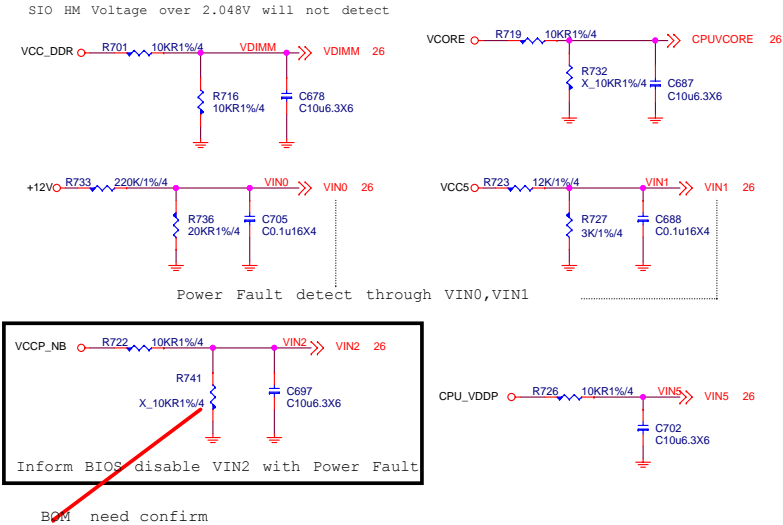
POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795	NAME	Circuit	NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE	UARTA80	ENABLE	UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE	UARTB80	ENABLE	UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE	TEST1MODE	ENABLE	TEST1MODE	LRESET
15	6793 test_point	6793 test_point	6793 NA	6793 NA	6793 NA	6793 NA	
15	6795 DDR4_EN	6795 DDR4_EN	6795 Disable	6795 Enable	6795 Enable	6795 Enable	
27	6793 DDR4_EN	6795 ESPI_EN	6793 Disable	6795 Enable	6793 Enable	6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS	2E	I/O ADDRESS	4E	LRESET
32	6793 TESTMOD2_EN	6795 FANOUT_DEF_EN	6793 disable	6795 default 50%	6793 Enable	6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE	Non_PORT80	ENABLE	PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE	INTEL DSW	ENABLE	INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE	AMD PWR SEQ	ENABLE	AMD PWR SEQ	RSMRST
103	TESTMODE_EN	WDT#	DISABLE	TESTMODE	ENABLE	TESTMODE	INTERNAL RSMRST

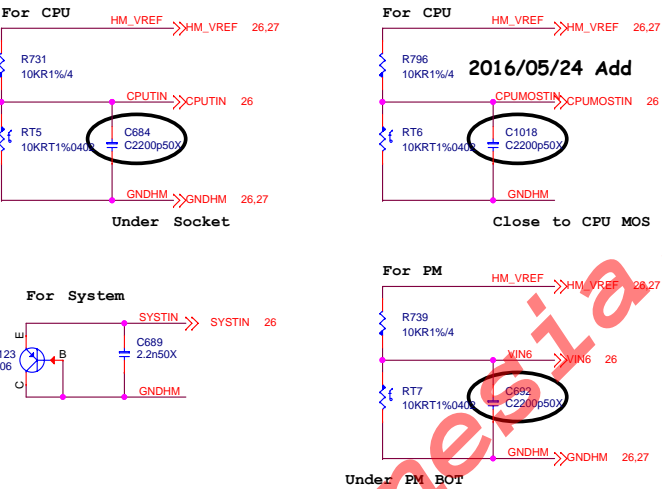
Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO



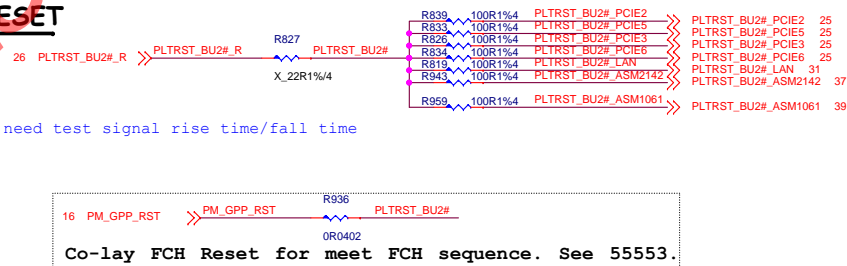
HW Monitor - Voltage



TEMP SENSOR

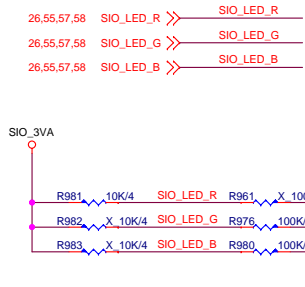


RESET

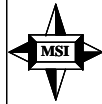


20161211 LED default Red

RGB LED default setting

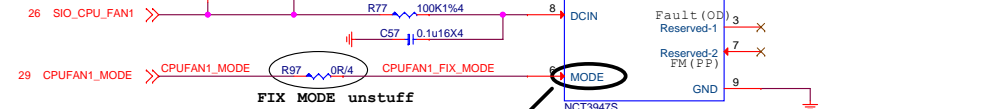


Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1



CPU_FAN1

From SIO



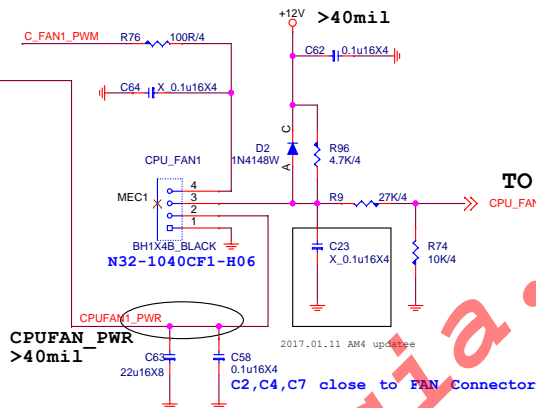
FIX MODE unstuff

GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

Internall pull up 1.65V

P/N:I22-3947S12-N62

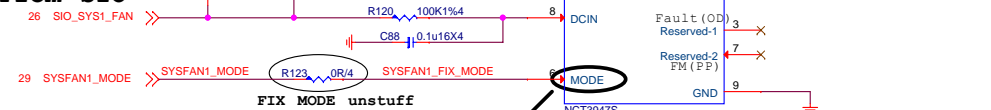


Avoid NCT3947S MODE PIN Leakage

Resever For FIX DC or PWM MODE USE By PM SPEC

SYS_FAN1

From SIO



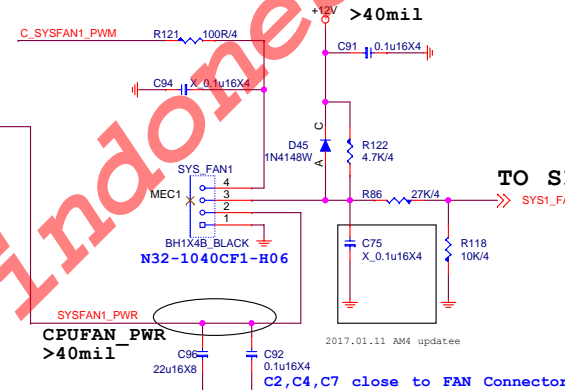
FIX MODE unstuff

GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

Internall pull up 1.65V

P/N:I22-3947S12-N62

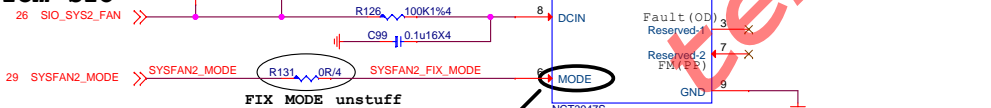


Avoid NCT3947S MODE PIN Leakage

Resever For FIX DC or PWM MODE USE By PM SPEC

SYS_FAN2

From SIO



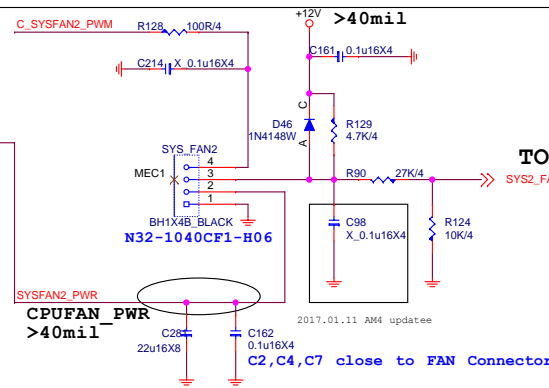
FIX MODE unstuff

GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

Internall pull up 1.65V

P/N:I22-3947S12-N62



Avoid NCT3947S MODE PIN Leakage

Resever For FIX DC or PWM MODE USE By PM SPEC



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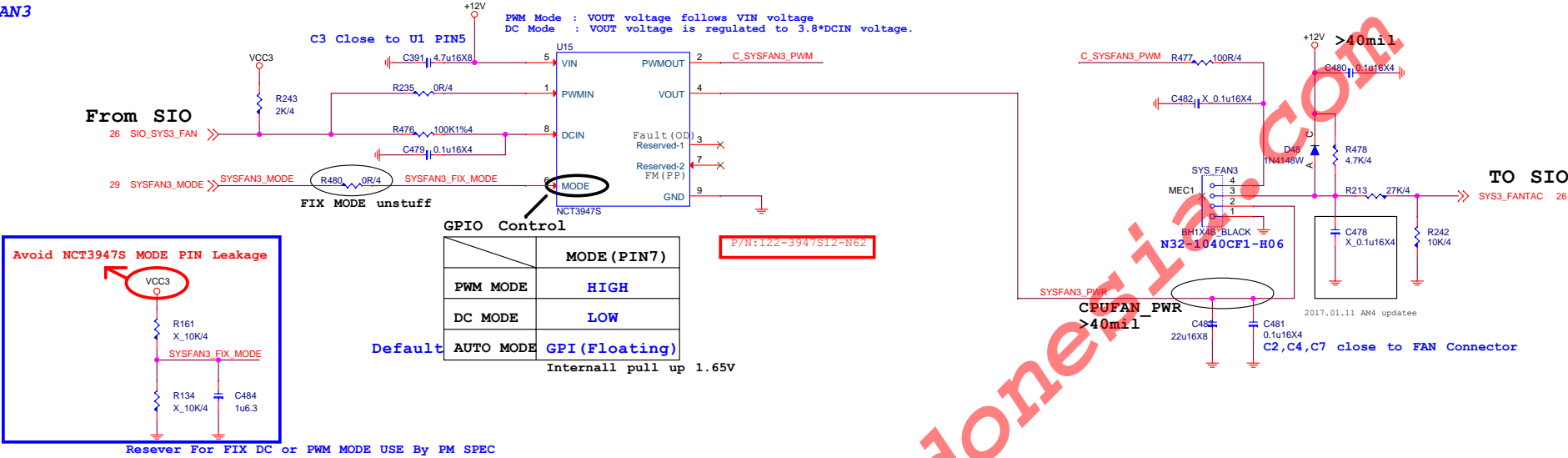
MS-7B00

Size	Document	Description	Rev
Custom	Document	CPUSYS FAN X2 TYPE K	11
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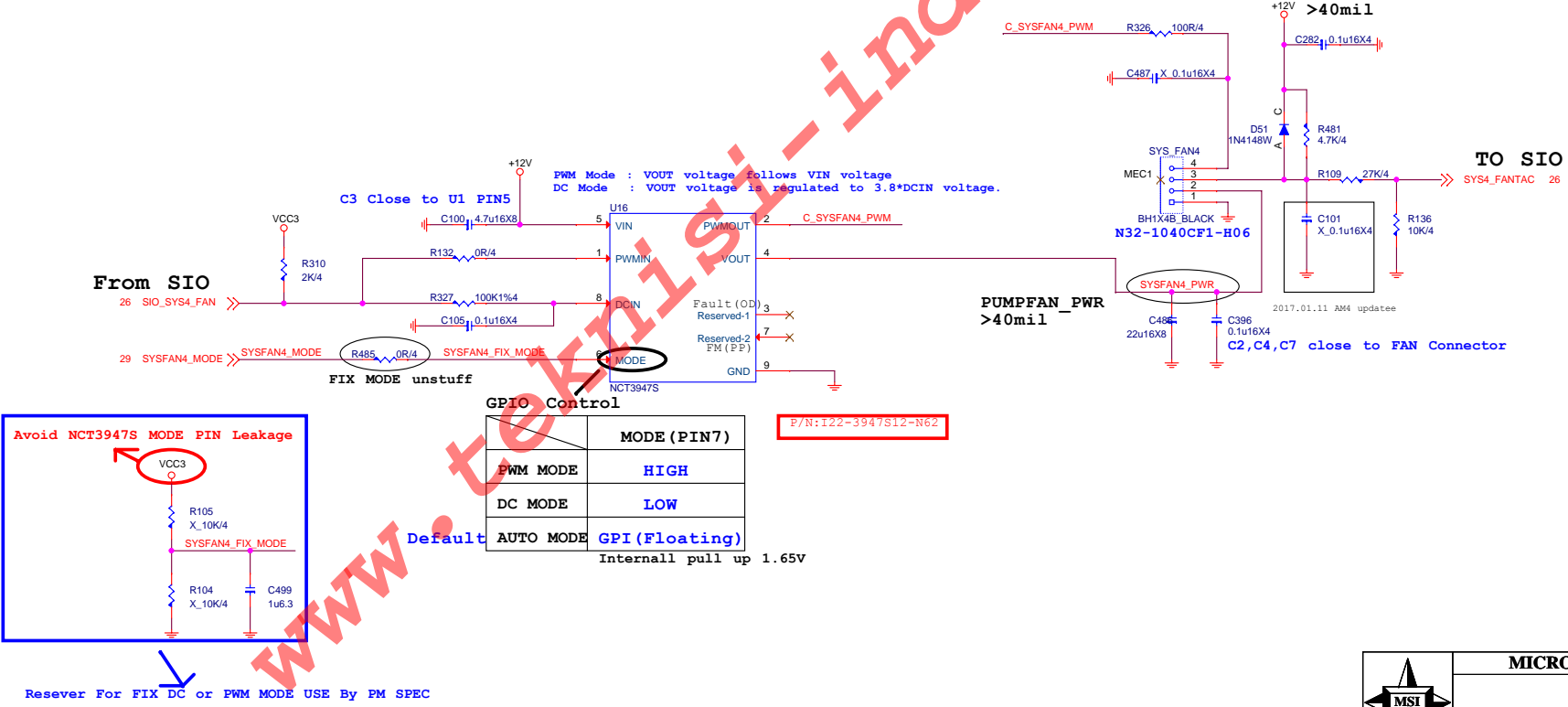
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO パッパ ち伝 PW M/DC M O D E

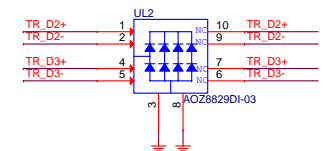
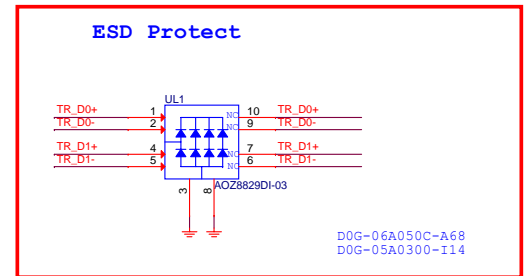
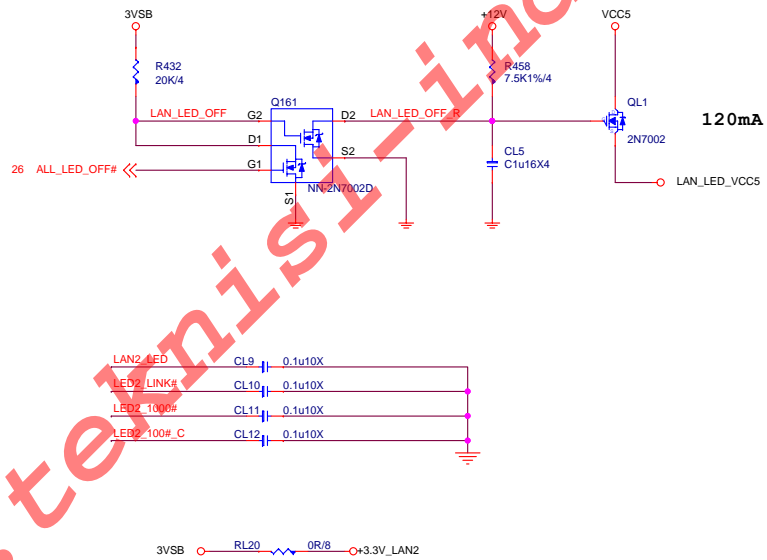
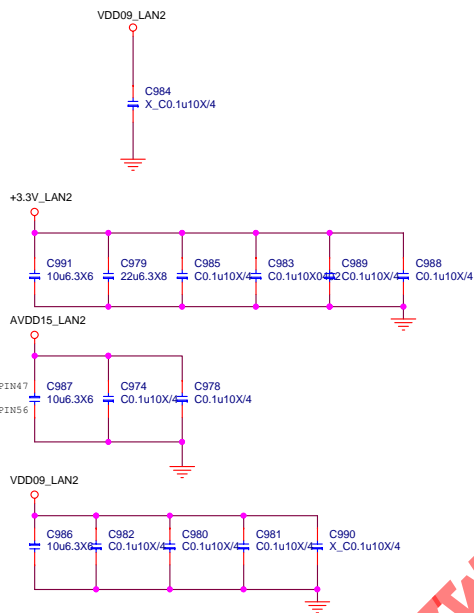
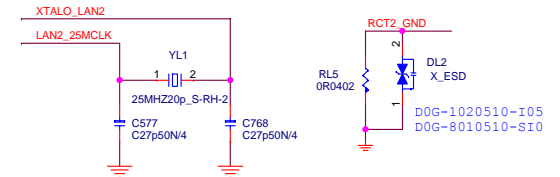
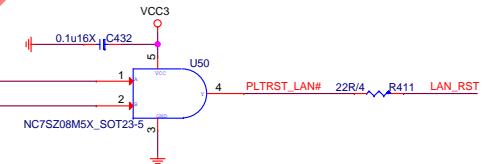
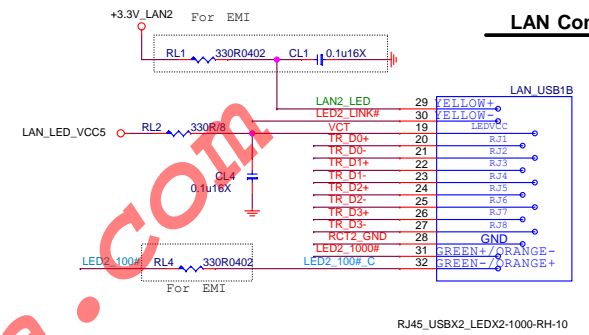
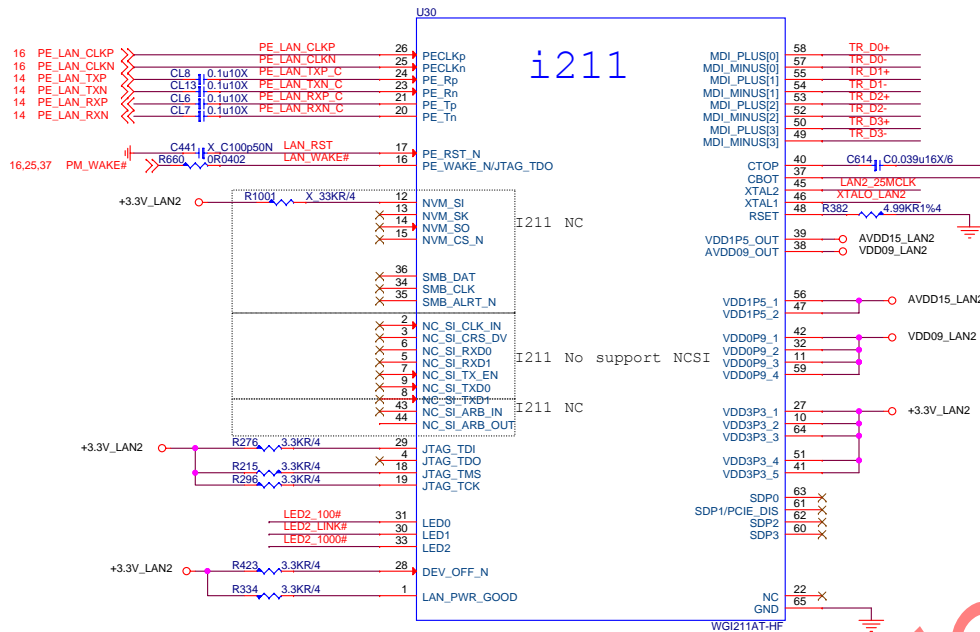
SYS_FAN3



SYS_FAN4



LAN2-- I211AT



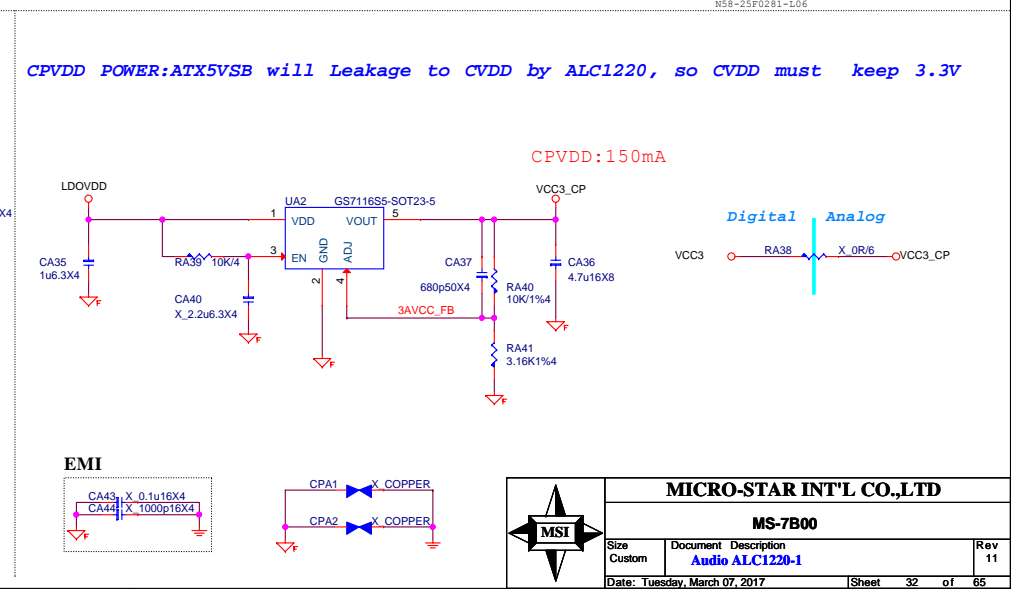
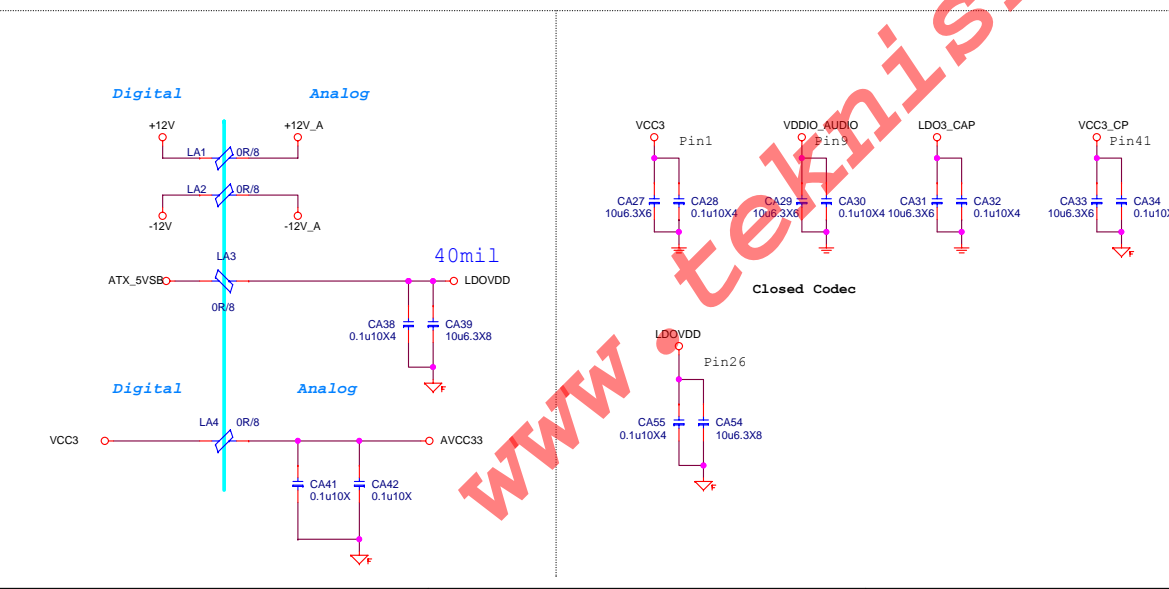
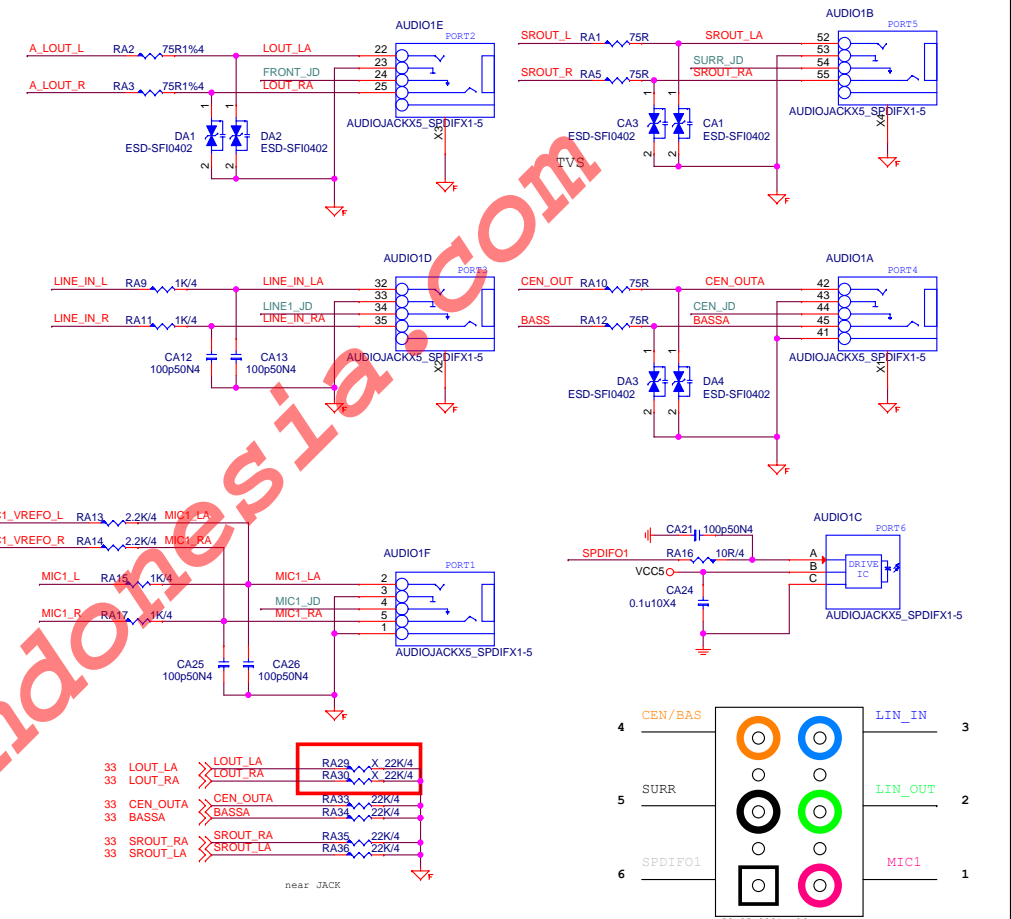
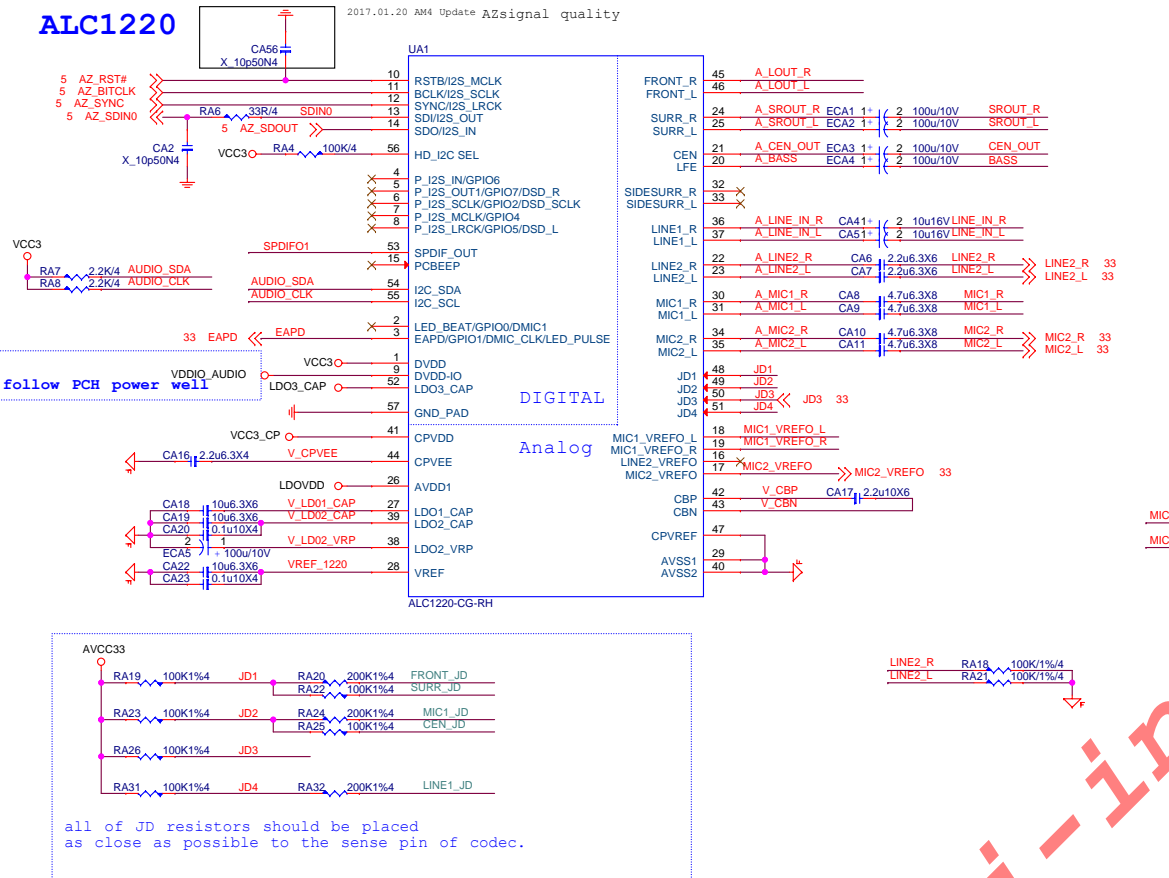
MICRO-STAR INT'L CO.,LTD

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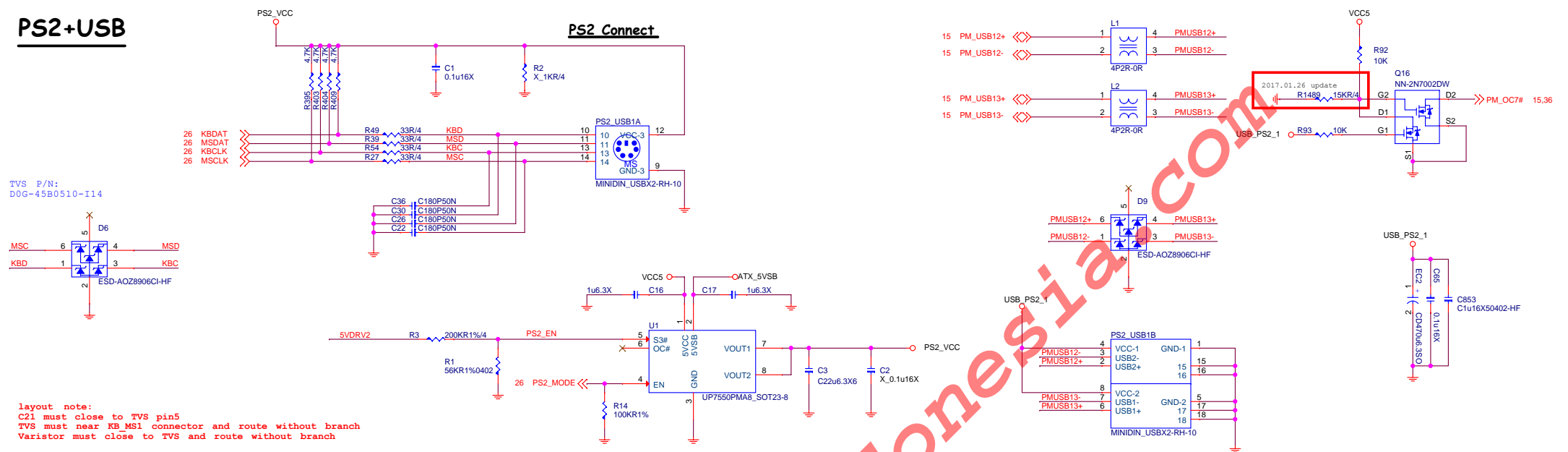
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ALC1220

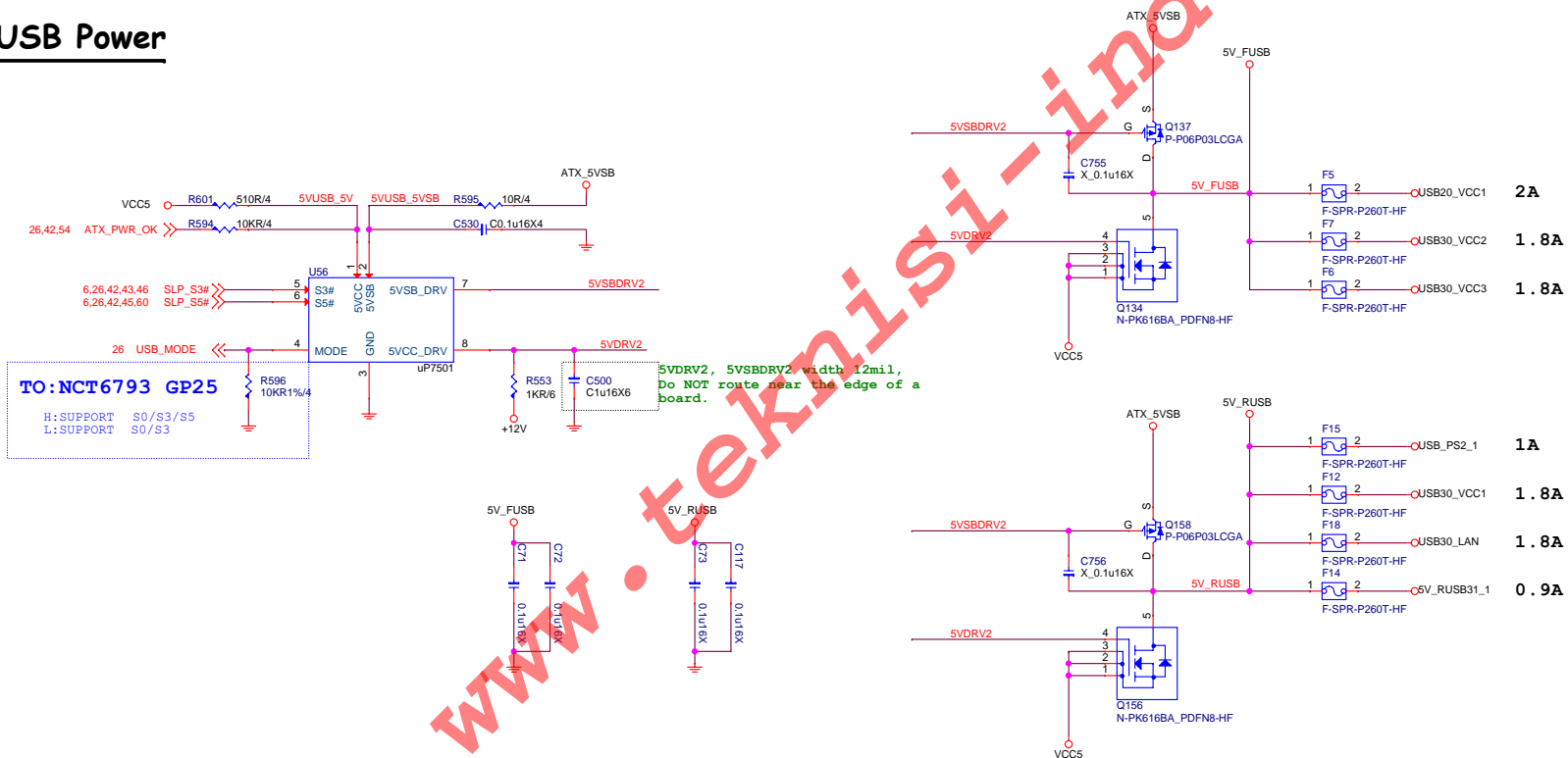
2017.01.20 RM4 Update AZsignal quality



PS2+USB



USB Power

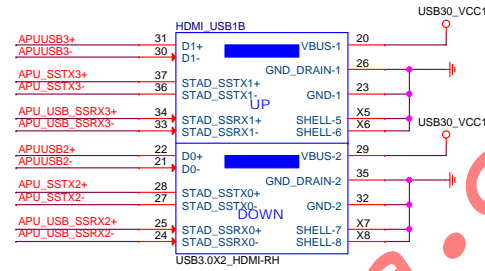
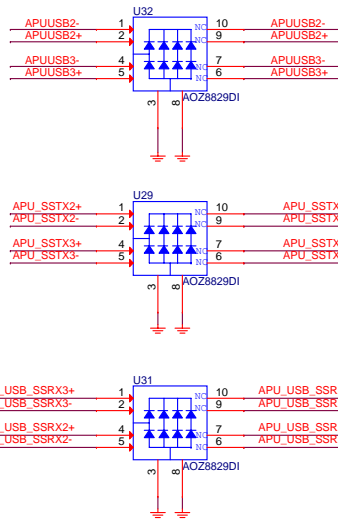
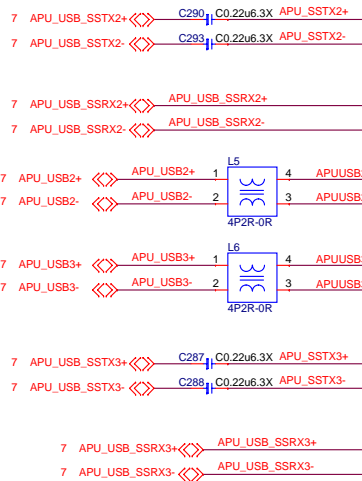


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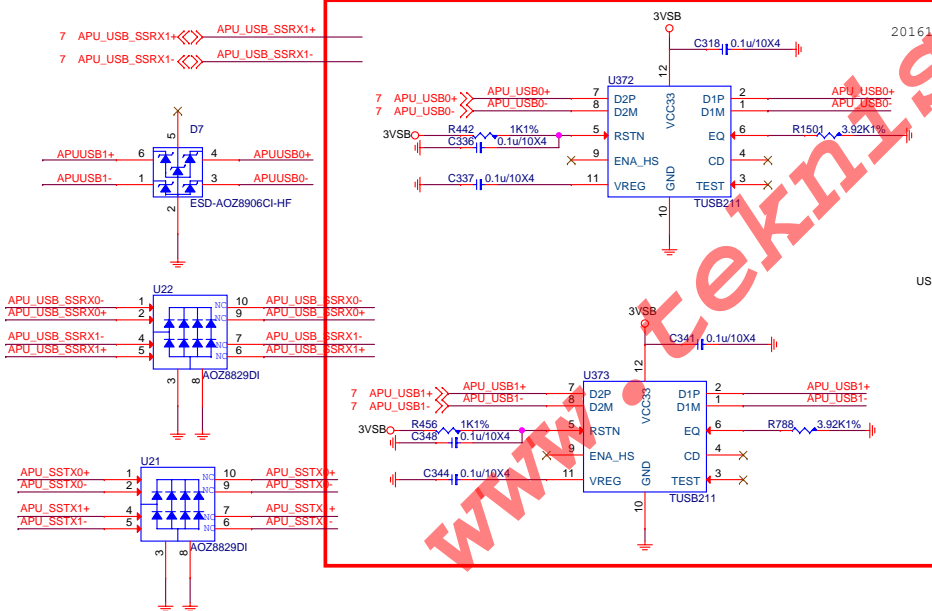
USB 3.0



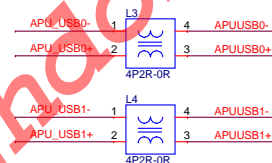
USB3.0



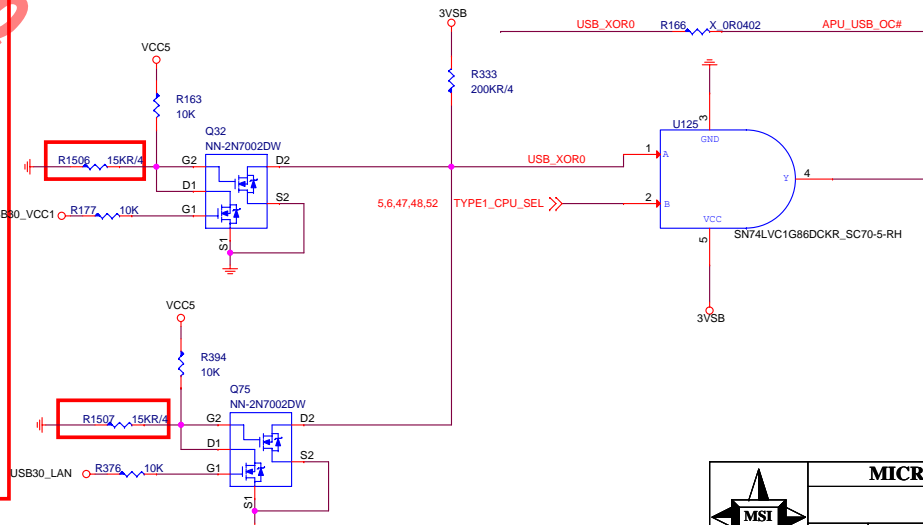
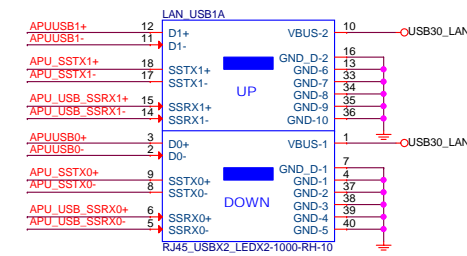
0205 update redriver signal



2016 1201 remover VR redriver



LAN+USB

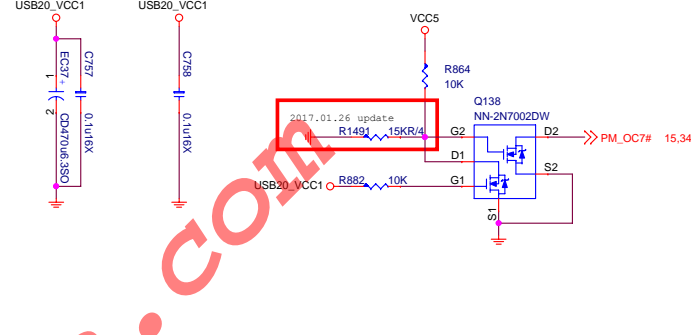
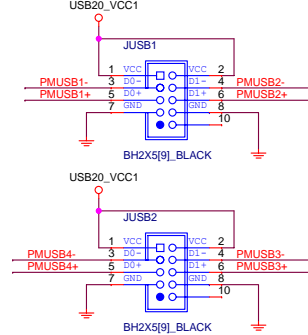
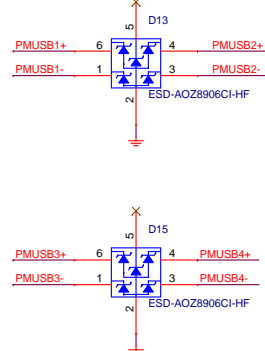
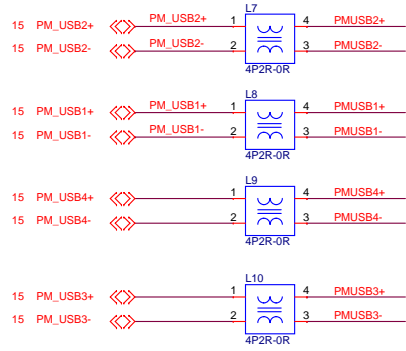


MICRO-STAR INT'L CO.,LTD

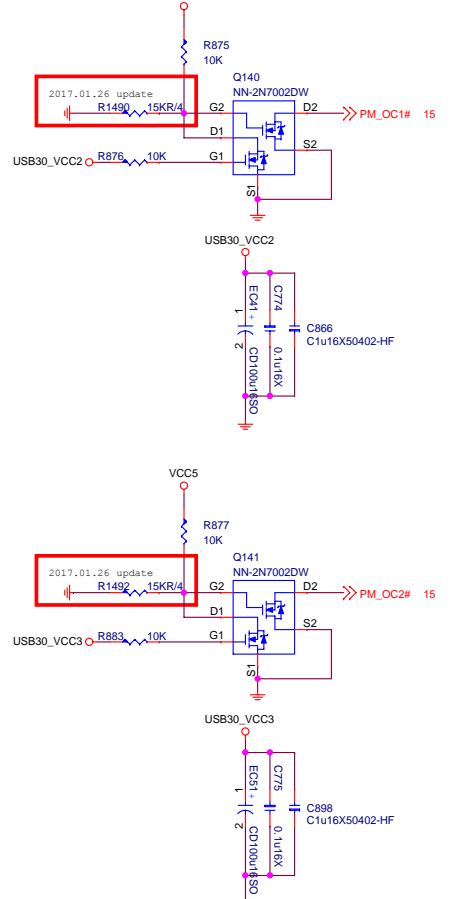
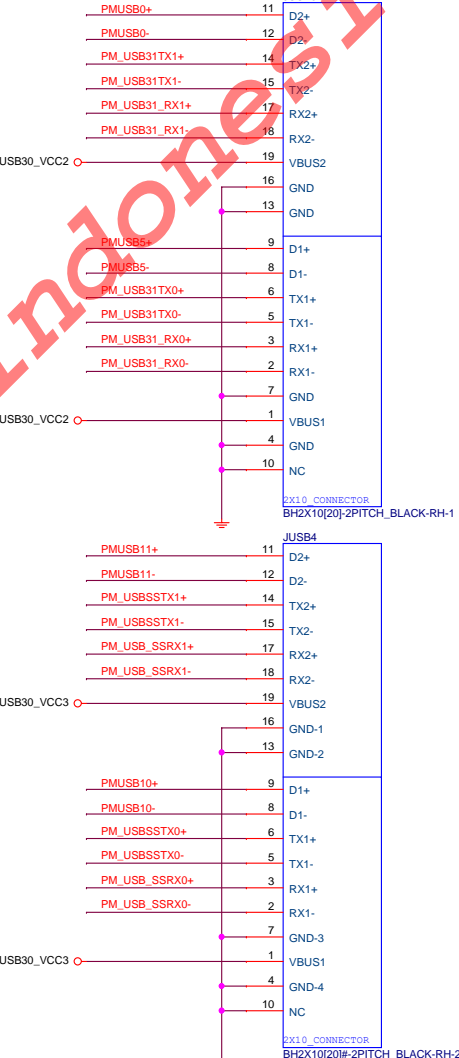
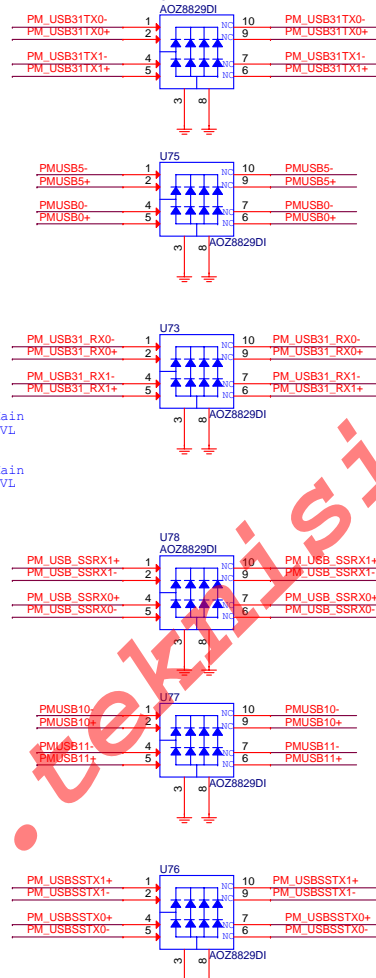
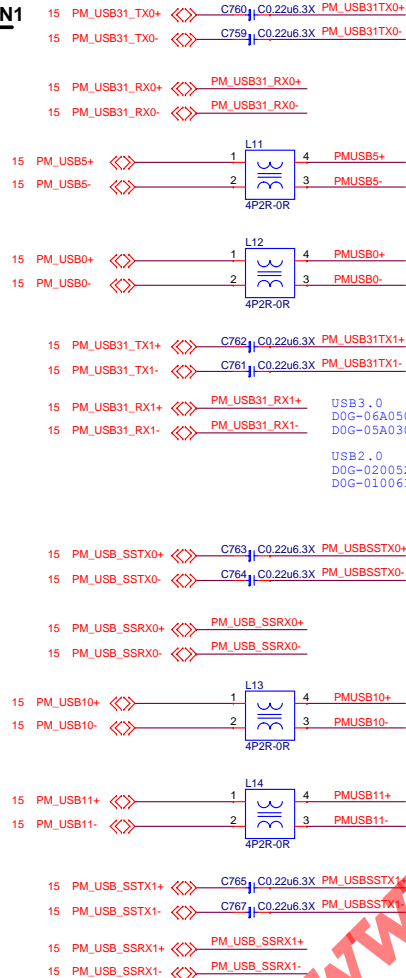
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Front USB2.0



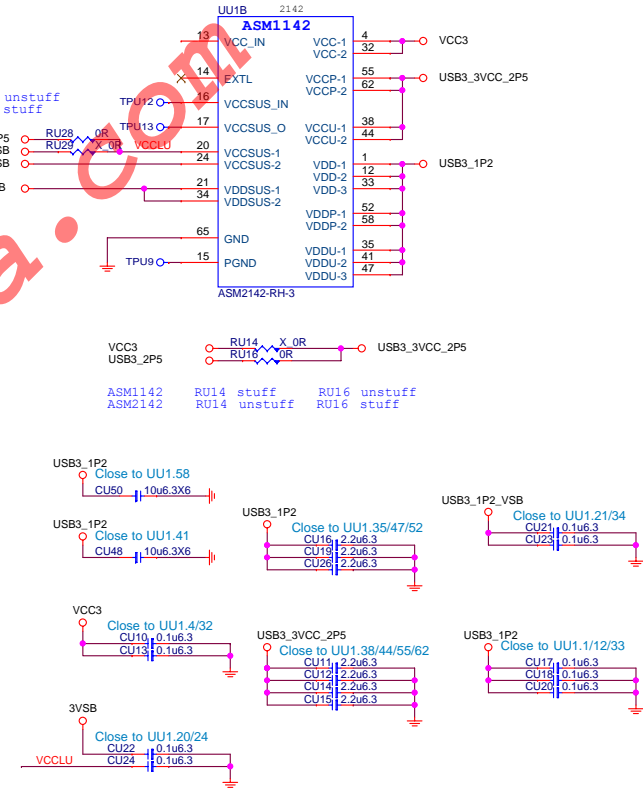
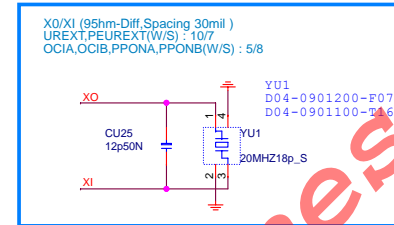
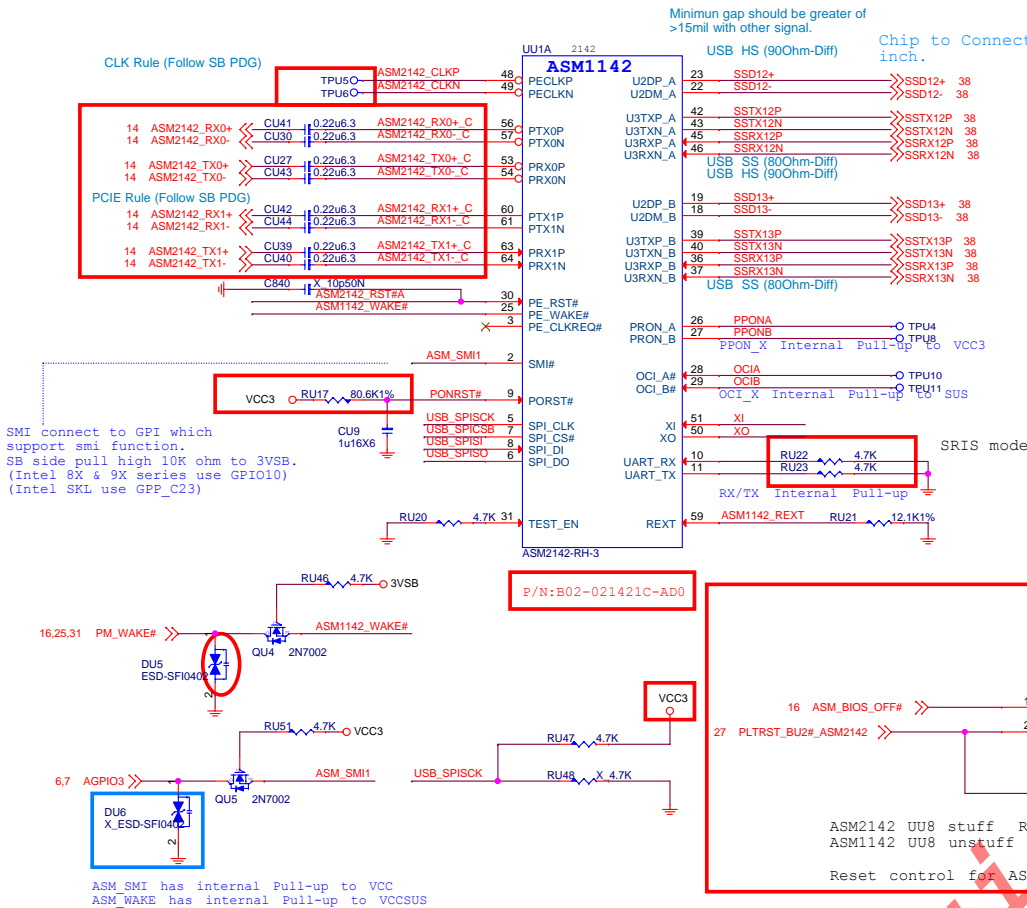
Front USB3.1 GEN1



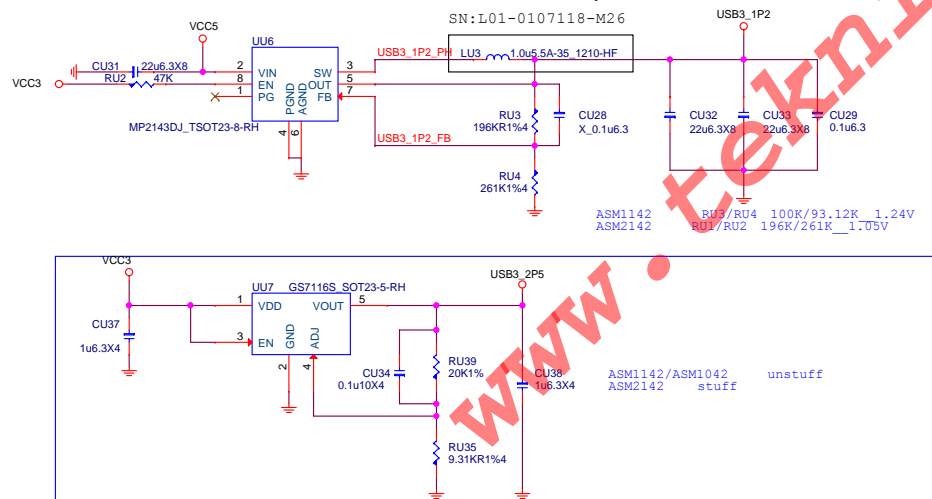
Power Consumption						
	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

Layout Guide:

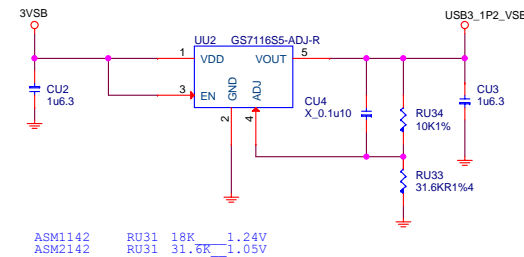
- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole <2



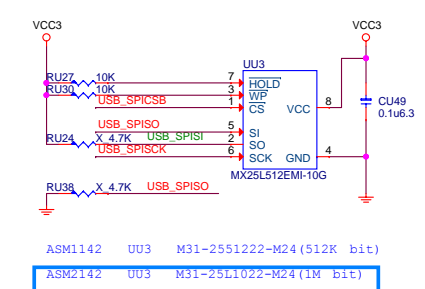
ASM1142 1.2 VCC Power



ASM1142 1.2 VSB Power



EEPROM



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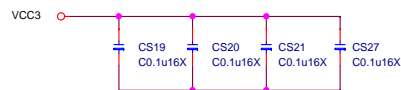
Size Custom	Document Description ASM2142 USB3.1	Rev 11
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SATA Connector

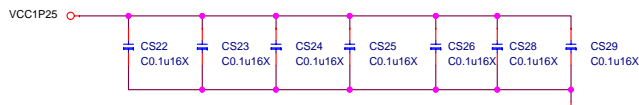
1.2V delay from 3.3V 90% > 0ms

ASM1061 POWER Consumption

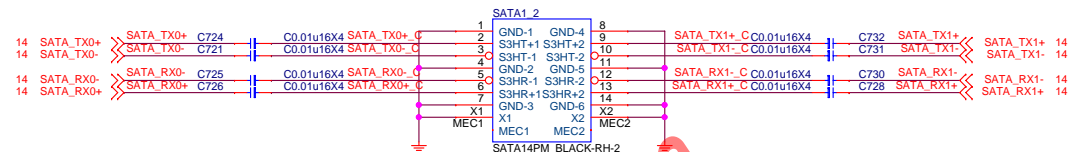
	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



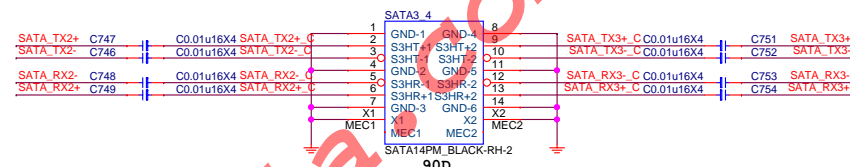
Place near pin 9,44,36,19



Place near pin 7,11,43,48,30,12,25



90D

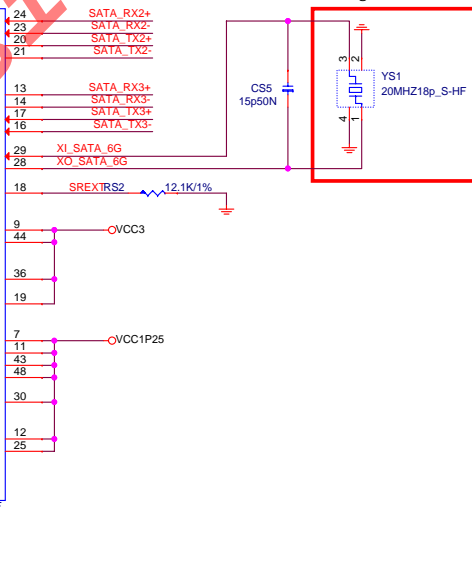
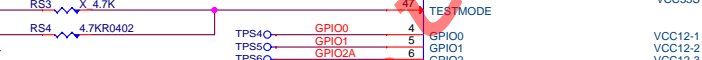
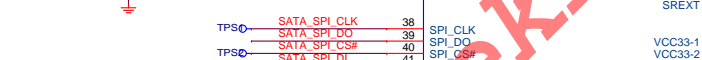
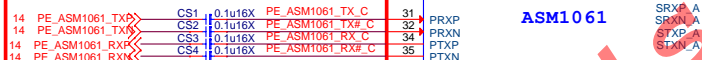


90D

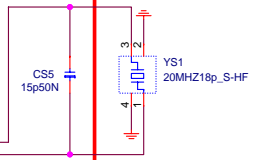
ASM1061 SATA6G

Add- 2012.02.20

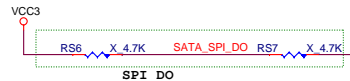
port0 1.2V delay from 3.3V 90% > 0ms
1. SATA 6G
2. SATA 6G
3. SATA 6G



change SMD



3.0



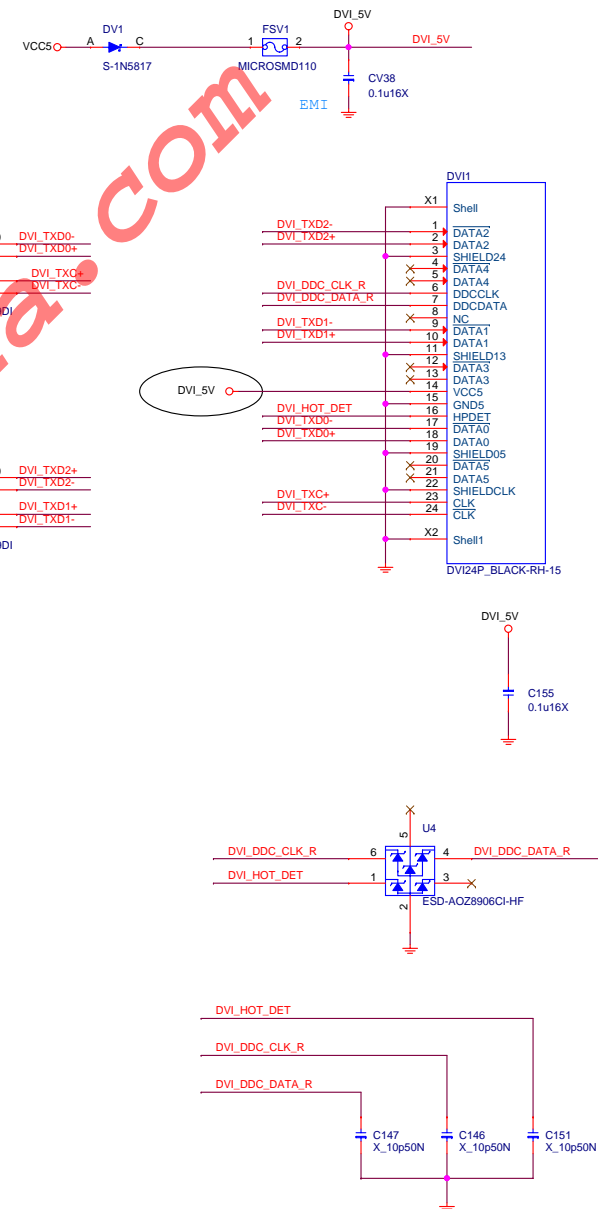
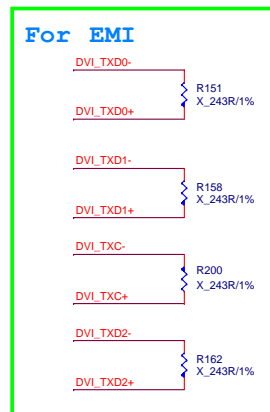
0: Spinup by H/W
1: Spinup by S/W

Add- 2011.3.18

SATA_SPI_DO don't need pull up (integrated pull-up)
or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

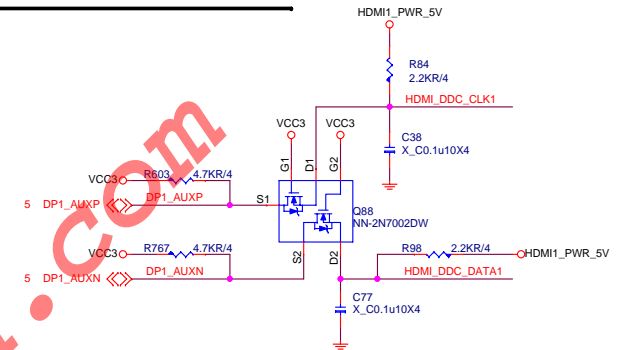


MICRO-STAR INT'L CO.,LTD

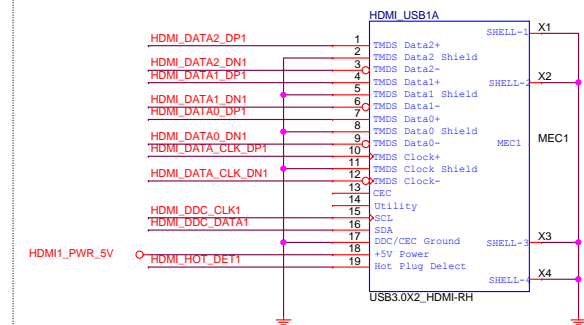
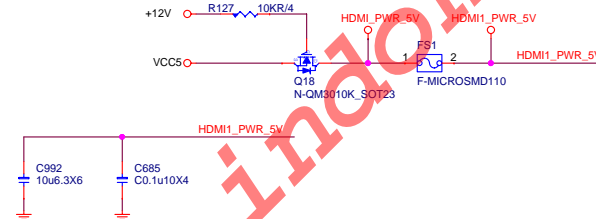
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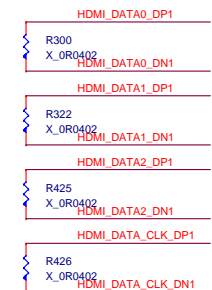
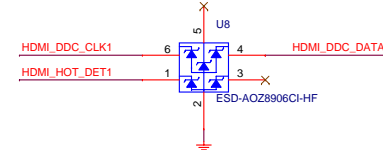
For HDMI 1.4



Connector Power



For EMI

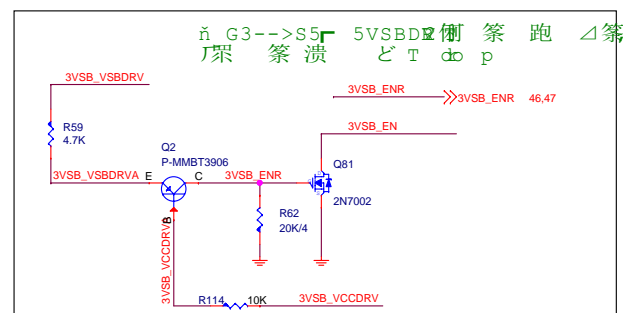
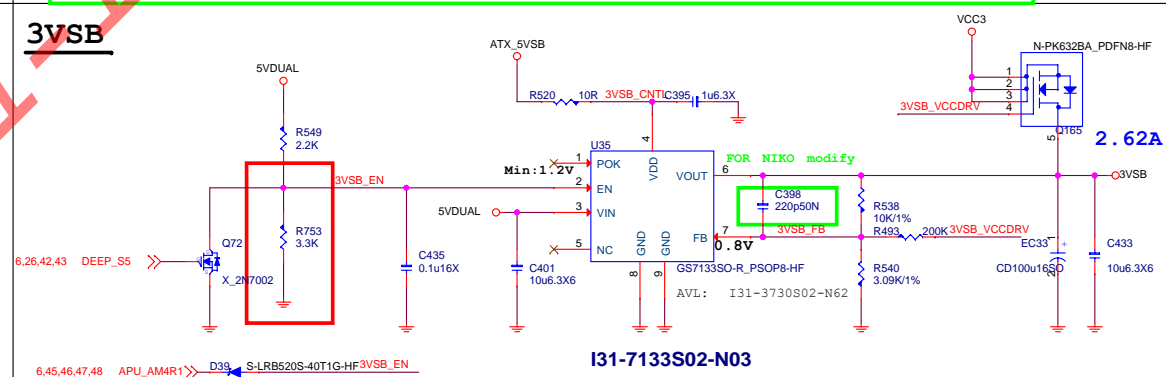
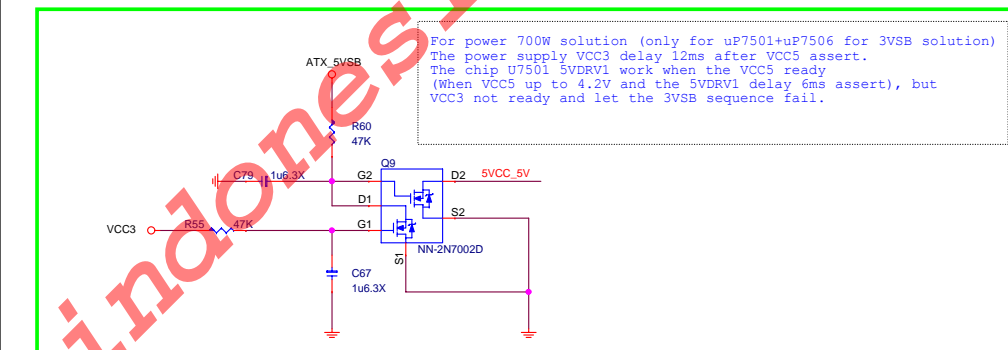


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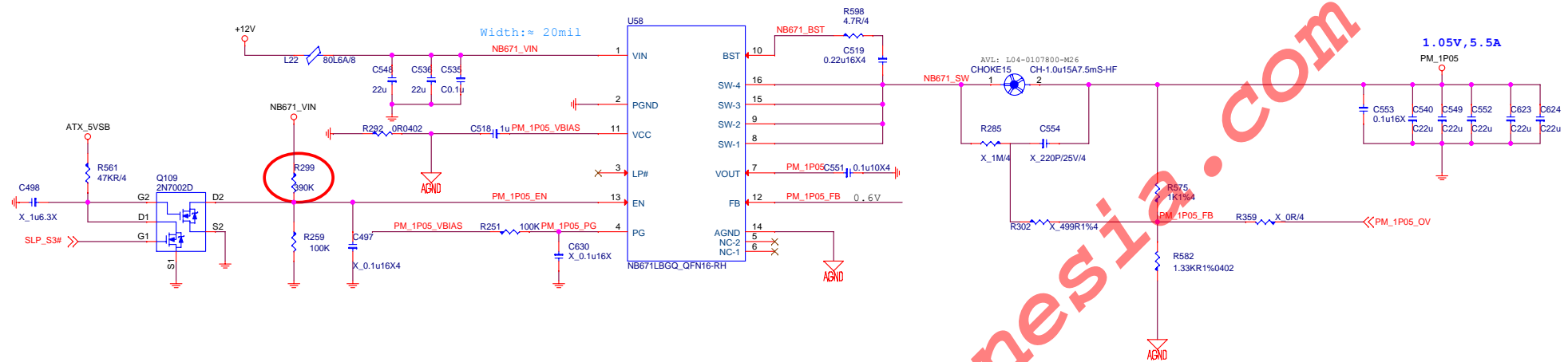
SIO_3VA



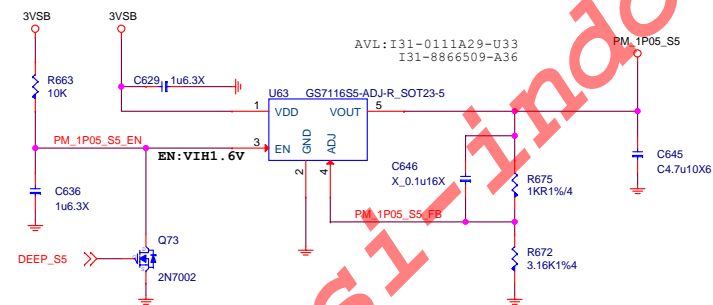
MICRO-STAR INT'L CO.,LTD			
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Size Custom	Document Description ACPI nPI-5VDIMM&3VSB		Rev 11
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$$0.7776 \mu H \leq 1.1664 \mu H$$

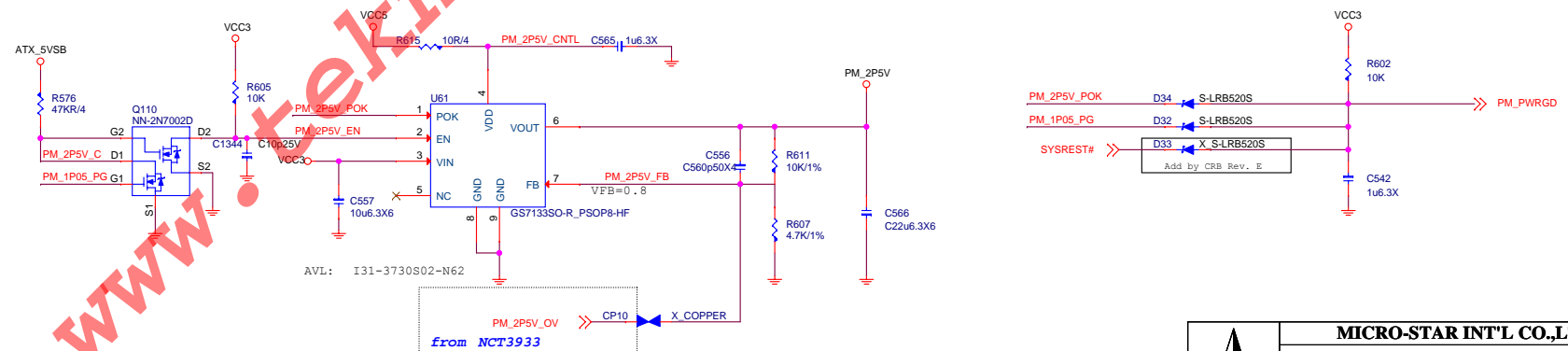
F: 500K



0.05A

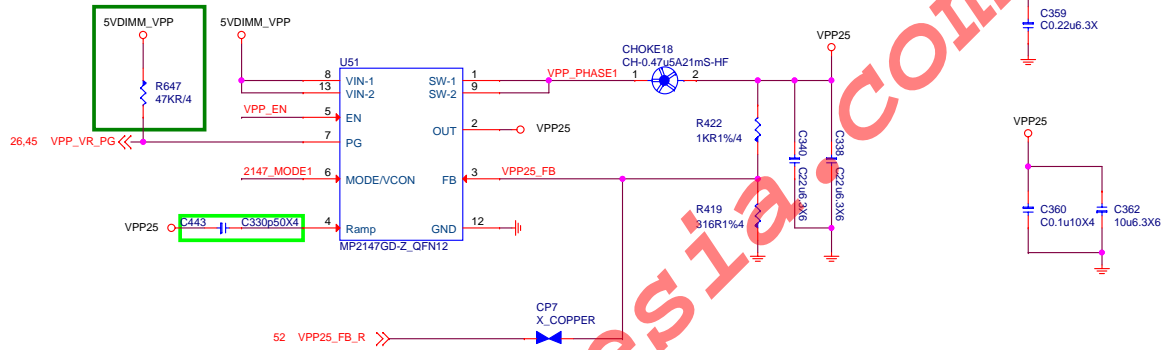
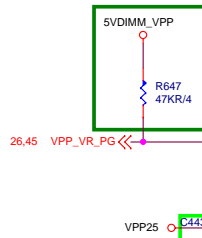


2.5V; 900mA

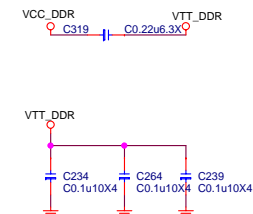
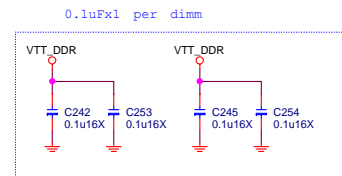
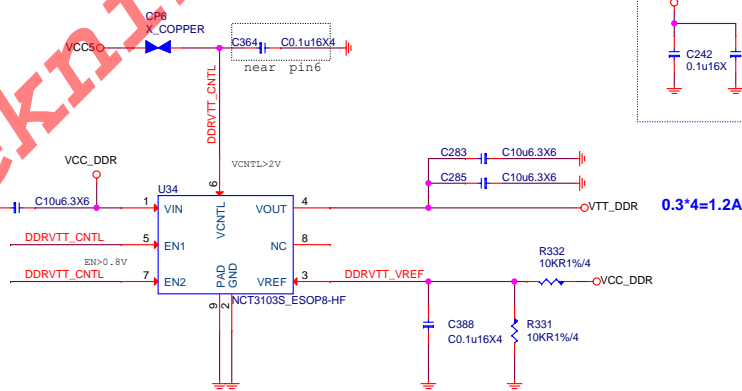


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To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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DDR4_1.2V 15.5A+9.5A+1.2A=26.2A

15.5A FOR CPU

9.5A FOR 2DIMM

1.2A FOR DDR VTT

VID	Reference Voltage (V)
H	0.675
L	0.75

Irms = Iout * SQRT(D/N- (D)^2)]
VCCDDR:
 $D = V_{out}/V_{in} = 1.2/5 = 0.24$
 $N = \text{Phase number} = 1$
 $= 26.2A * \text{SQRT}(0.24 - 0.0576)$
 $= 11.2A$

OCP:35A
Imax: 26.2A

HW default 1.36V
JOV1 jump 1.4V
BIOS porting SPD voltage

uP1504 & RT8125
VCC Input Range : 4.5V to 13.2V

2015.07.14 Add +12V loading

2015.07.14 update to 0603

$V_{out} = 0.8V * (1 + R70/R79) = 0.8V * (1 + 1k/2.15k) = 1.172V$

FB: 0.8V
 $V_{out} = 0.8 * (1 + R1/R2)$

MAX: 20.85A

1.2V

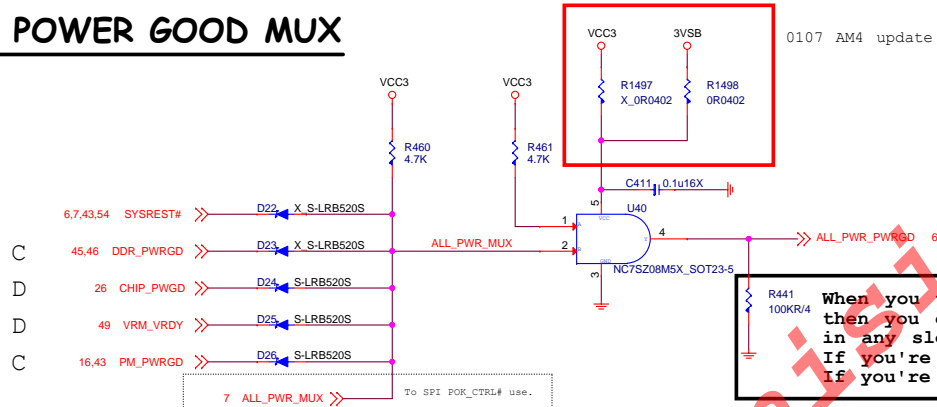
VCC_DDR
VTT_DDR

OCP=35A
OCPSET:min 5Kohm
OCP
 $= (R232 * 10uA) / R_{dson}$
 $= (R232 * 10uA) / 3.3m/2$
 $= 35A$

R232=5.775k

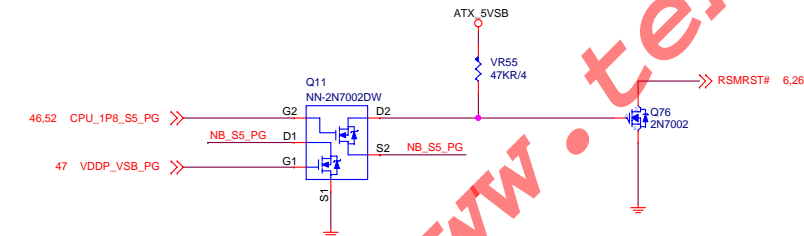
MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7B00			
Size	Document	Description	Rev
Custom		DDR Power-RT8125E	11
Date: Tuesday, March 07, 2017		Sheet 45 of 65	

ALL POWER GOOD MUX

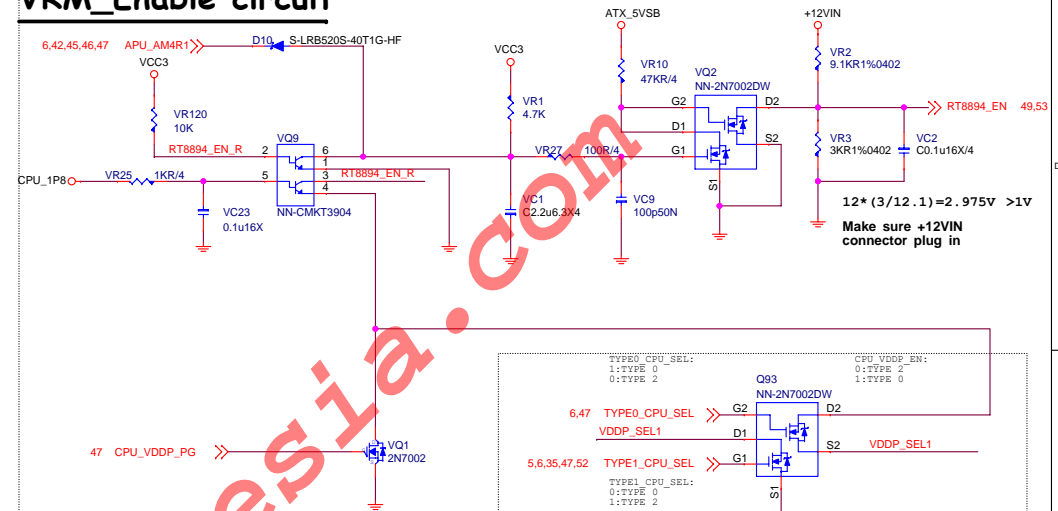


S0 PG

S5 PG



VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	0	0	0
SR	2	1	1
RV/ZP	3	1	0



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Size	Document	Description	Rev
Custom		CPU Power Connector/PWRGD	11

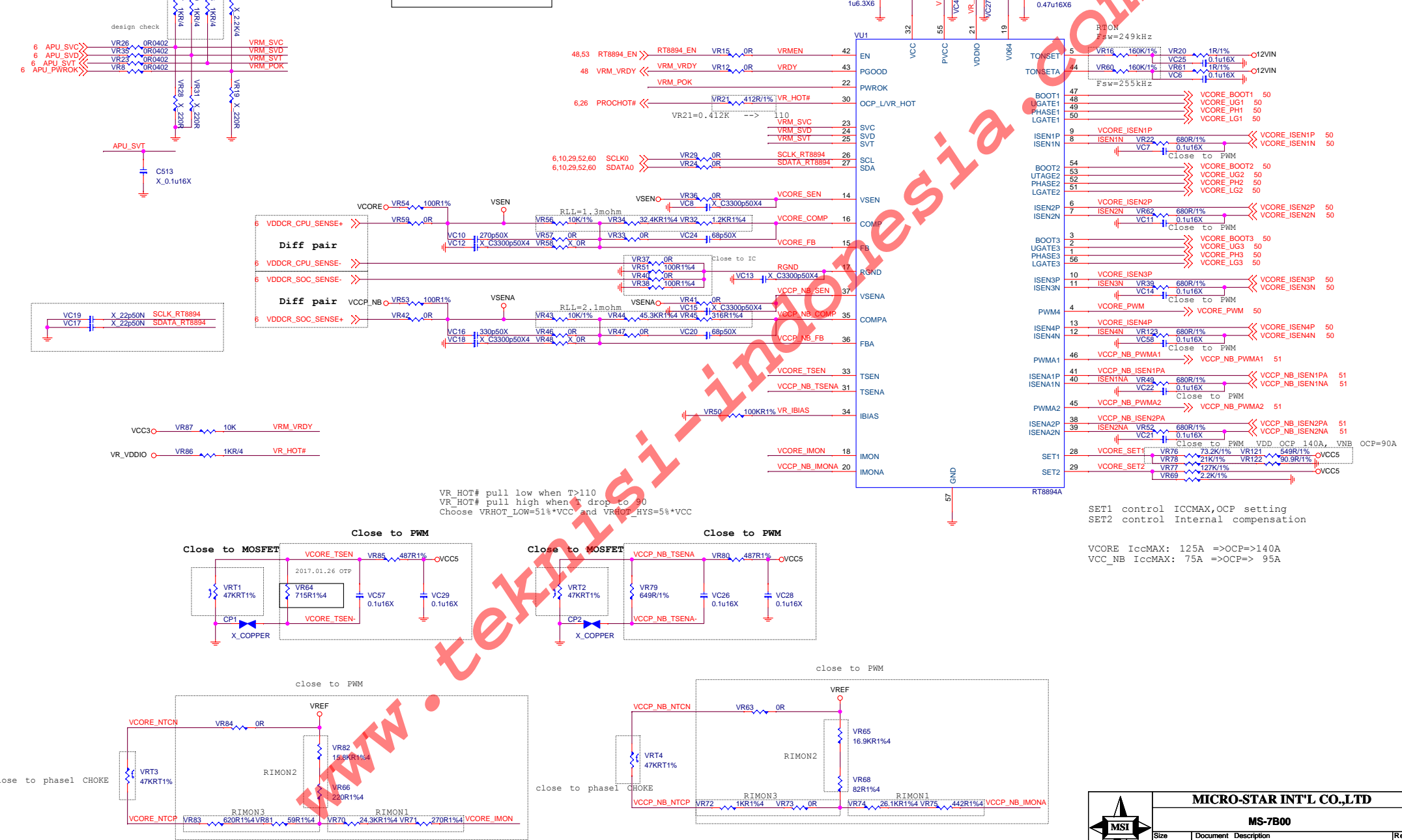
Date: Tuesday, March 07, 2017 Sheet 48 of 65

Note:VID Override Circuit

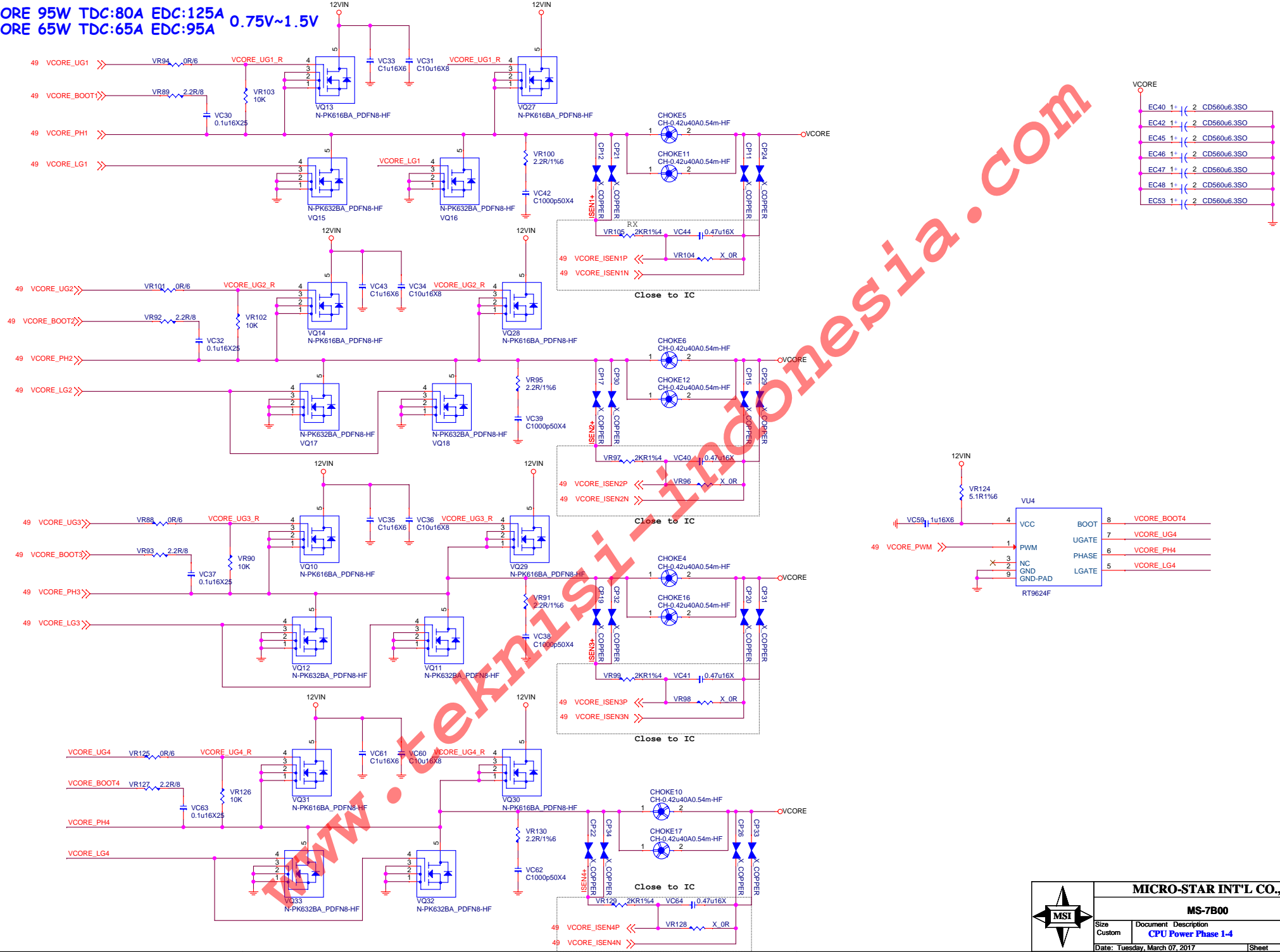
BOOT VOLTAGE		Pre_PWROK Metal VID	
SVC	SVD		
0	0	1.1	
0	1	1.0	
1	0	0.9	
1	1	0.8	

2017.01.20 AM4 Update

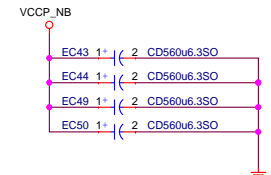
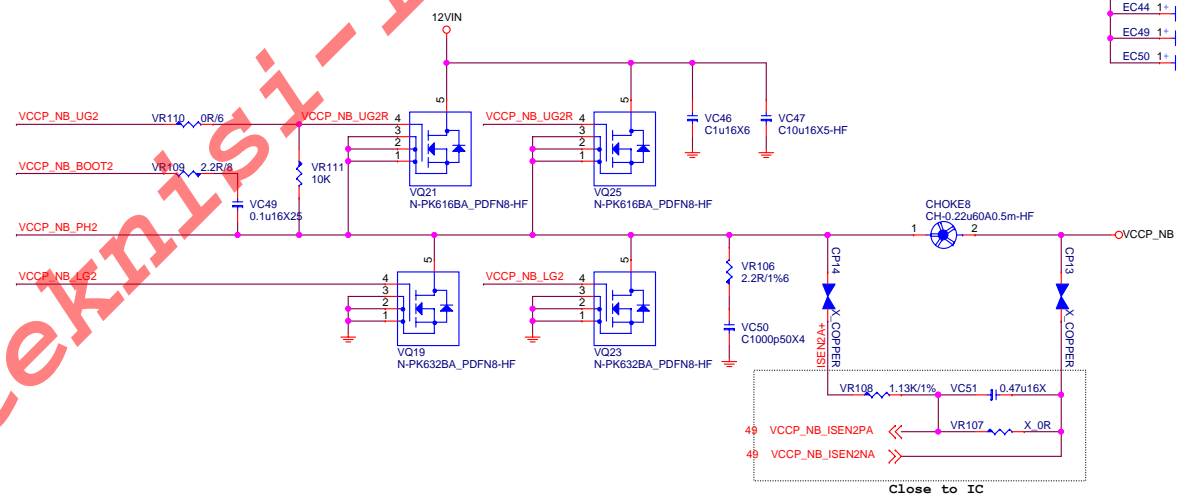
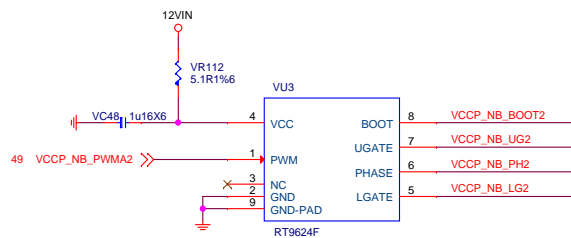
Remvove J5MB1



VCORE 95W TDC:80A EDC:125A 0.75V~1.5V
VCORE 65W TDC:65A EDC:95A



0.75V~1..2V



MS-7B00

Size Custom	Document Description CPU Power NB Phase 1-2	Rev 11
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FOR VCCP_SOC_S5 0.9A

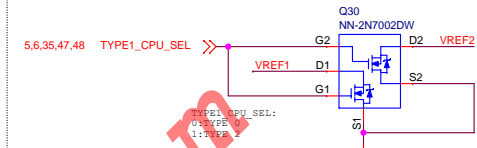
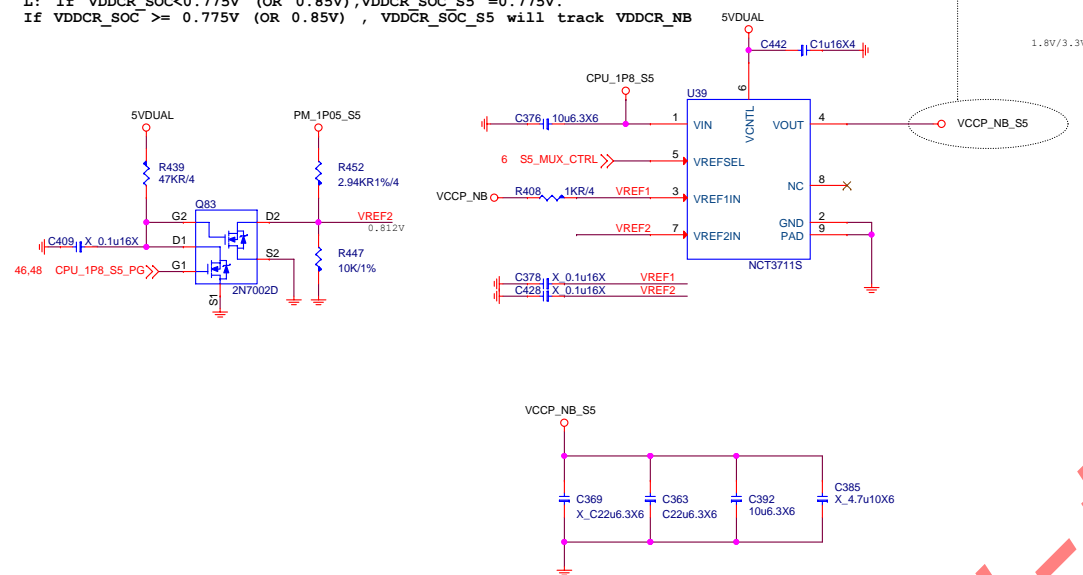
TYPE0 Only

S5_MUX_CTRL
HIGH: S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

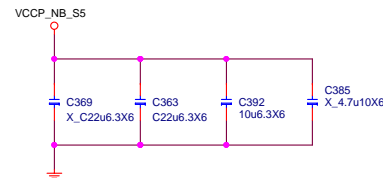
(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)

Bristol Ridge TYPE0

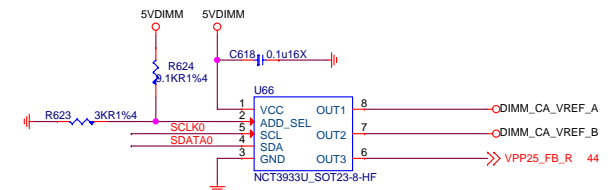


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0



0x28: RH=9.1K, RL=3K

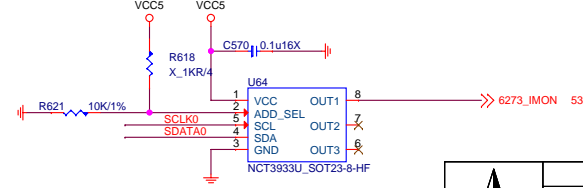
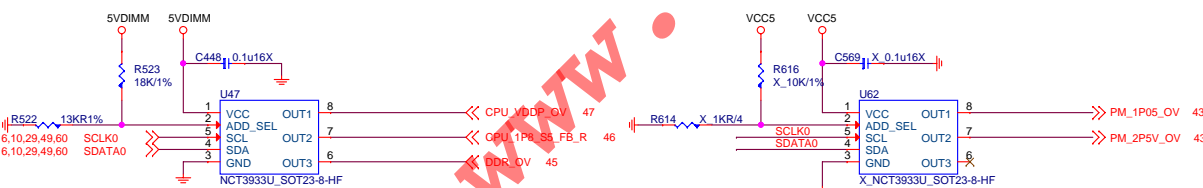


Over Voltage Control IC

0x26: RH=18K, RL=13K

0x20: RH=10K, RL=OPEN

0x2A: RH=OPEN, RL=10K



UPI VOLTAGE CONSOLE

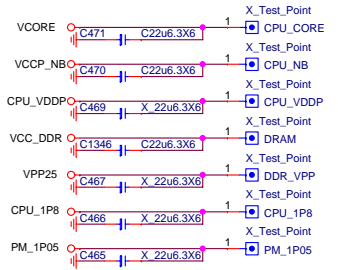
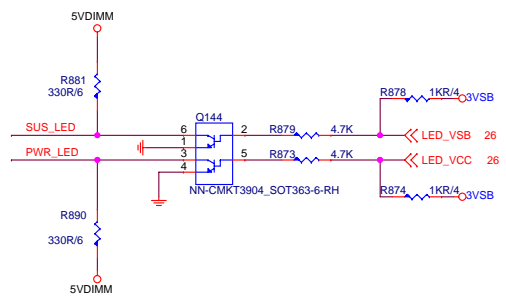
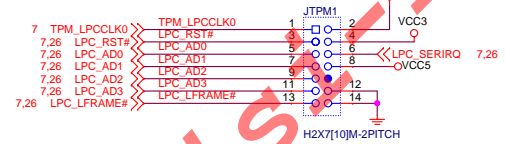
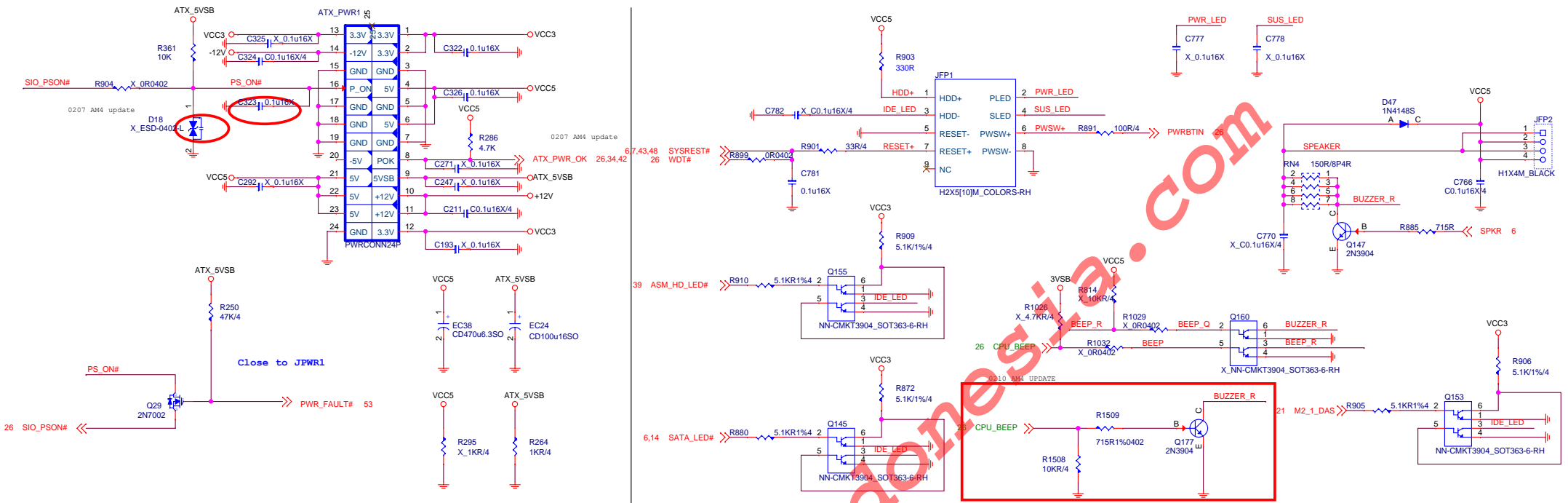
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



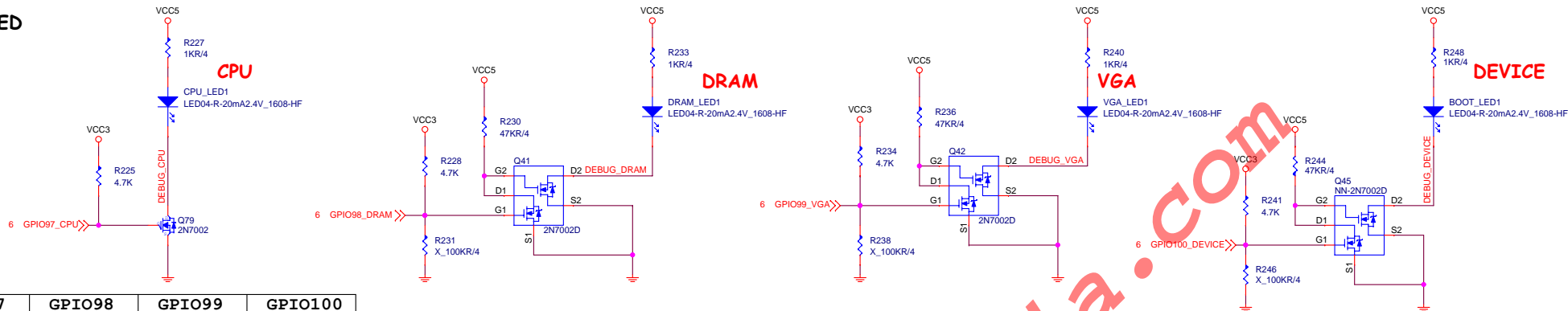
MICRO-STAR INT'L CO.,LTD

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Size	Document	Description	Rev
Custom	Document	CPU Power NB Switch/NCT3933	11
Date: Tuesday, March 07, 2017	Sheet	52 of 65	

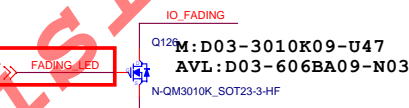
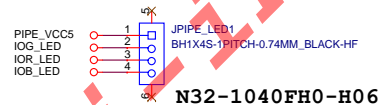
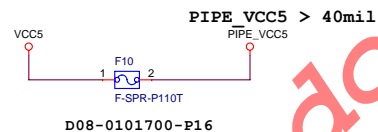
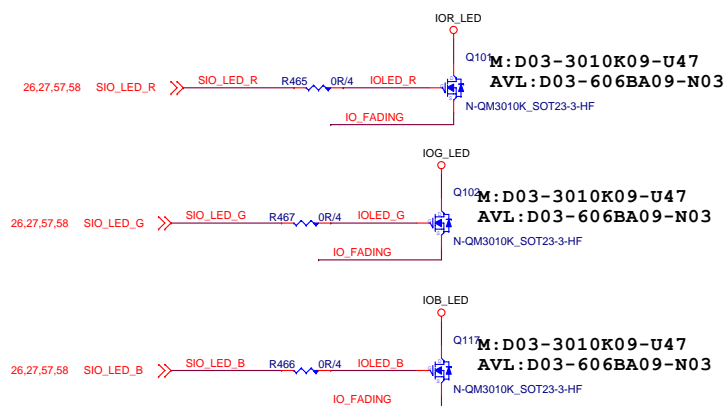


EZ Debug LED



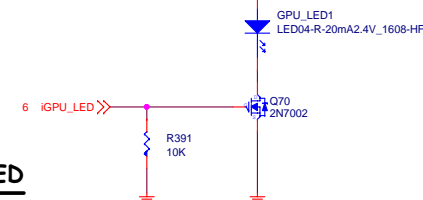
GPIO	GPIO97	GPIO98	GPIO99	GPIO100
LED	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

IO Cover RGB LED

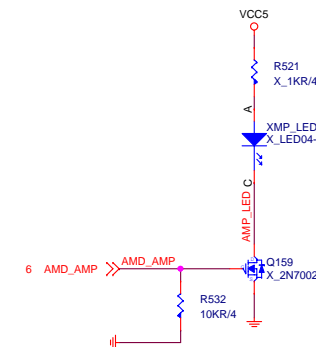


AM4 APU Detect LED Circuit

iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON



AMD AMP Detect LED



LED	x16	x8	x4
PCIE2	Red	White	White

GPIO	EGPIO95	EGPIO96
LED	GPI PO HIGH	GPI PO HIGH
防滅	GPI (default LOW)	GPI (default LOW)



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Size	Document	Description	Rev
Custom		EZ-Debug LED Control	11
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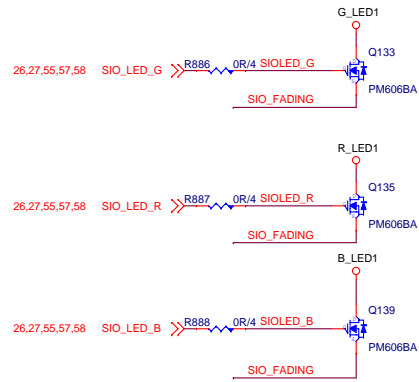


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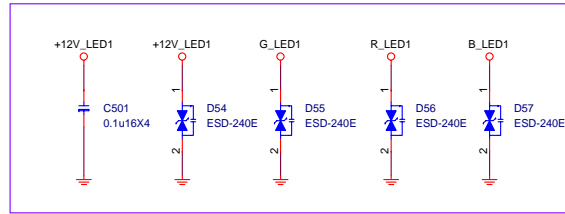
MS-7B00

Size Custom	Document Description NO Circuit2	Rev 11
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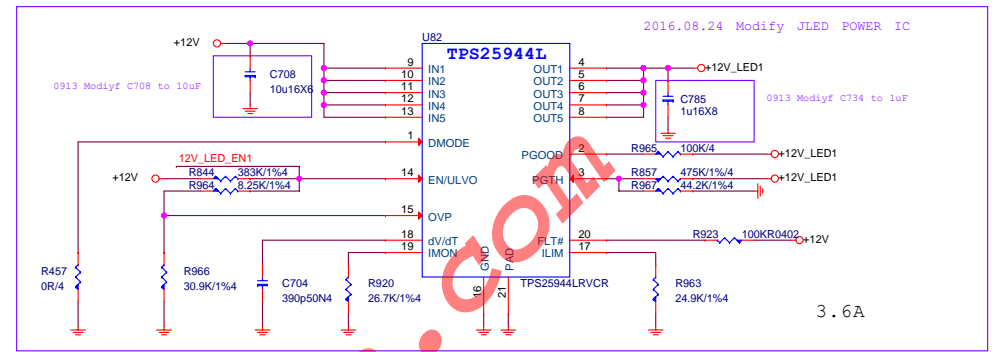
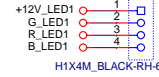
LED STRIPLINE(LEFT)



2016.08.24 Add,Close to JLED1



20161211 SIO_MLED



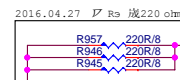
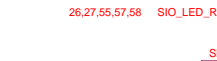
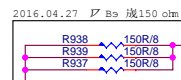
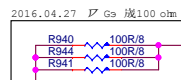
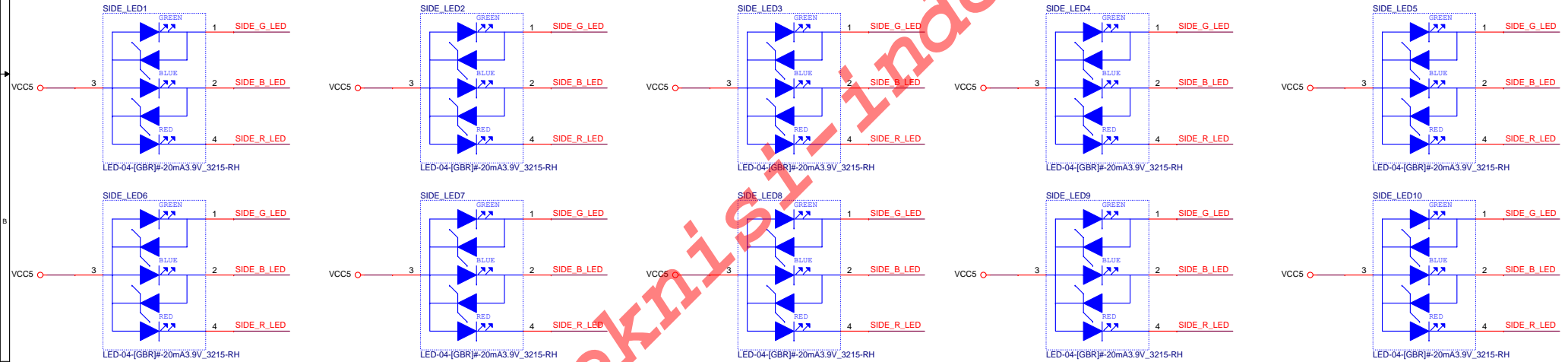
锁LE 鎰兵 (RG B)

PCB 球 (JLED1)

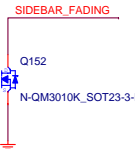
も 参 頤 や穿 夹非 505 B GB LED 鎰兵 (1 鎰兵羅 块 篆球 綜 歲 3 蚌 (12 工 疚) ,

繼 姿へ 沉 7 A 2 0 噴 靠

BOARD SIDE LED



20161211 SIO_MLED



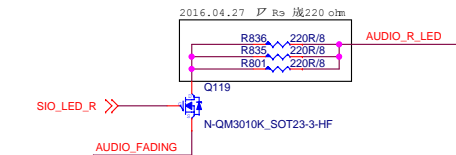
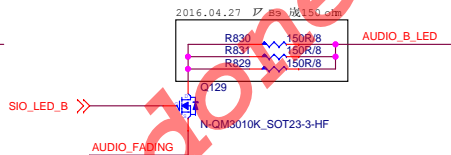
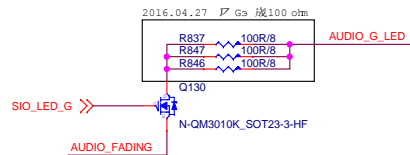
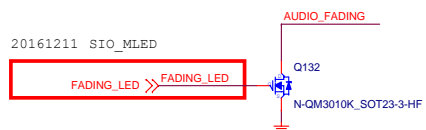
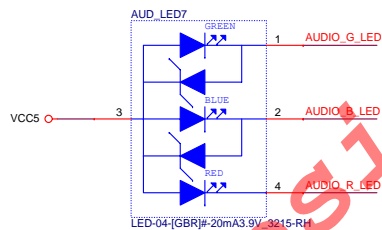
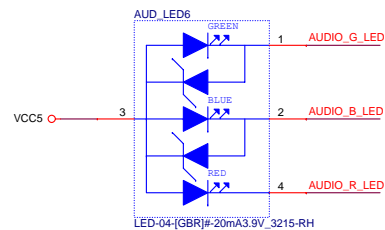
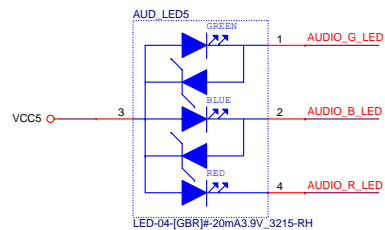
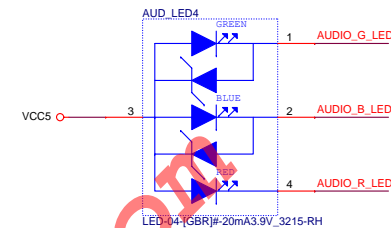
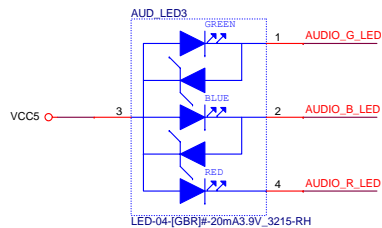
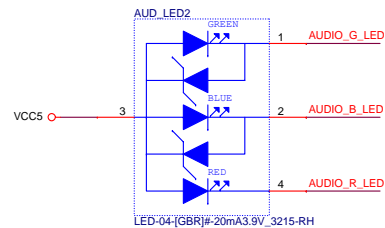
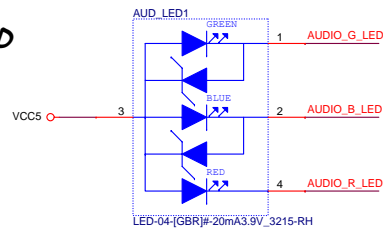
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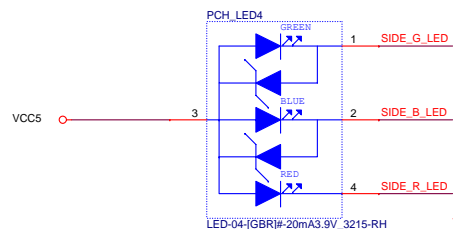
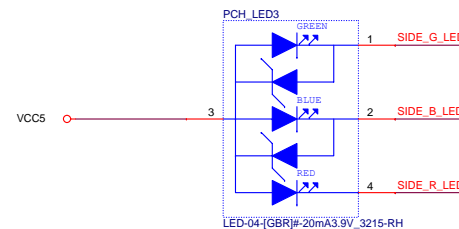
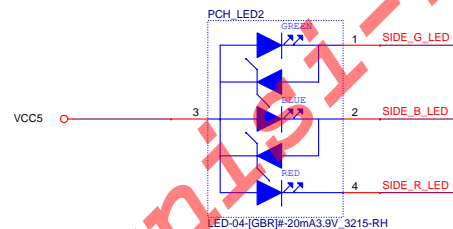
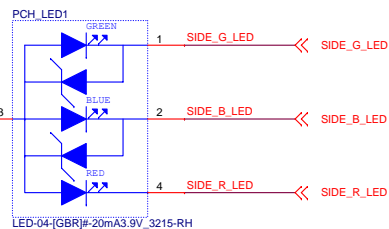
Size	Document	Description	Rev
Custom		LED STRIPLINE	11
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AUDIO_MOAT LED

LEFT

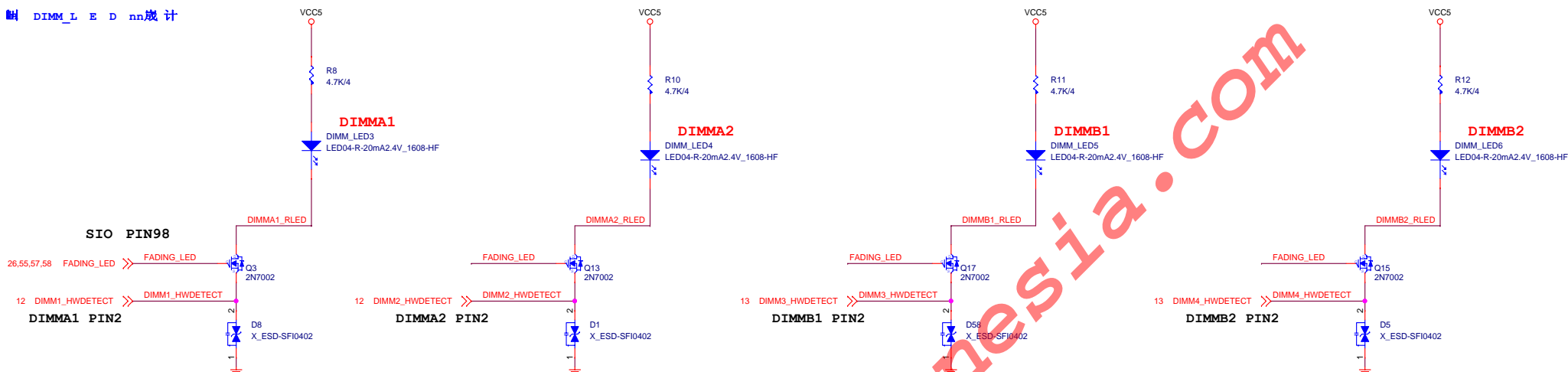


PCH LED

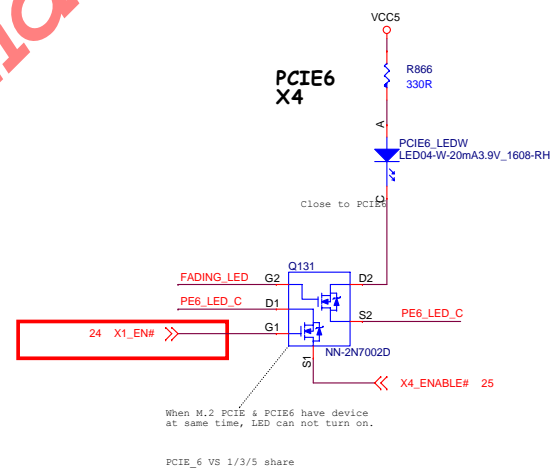
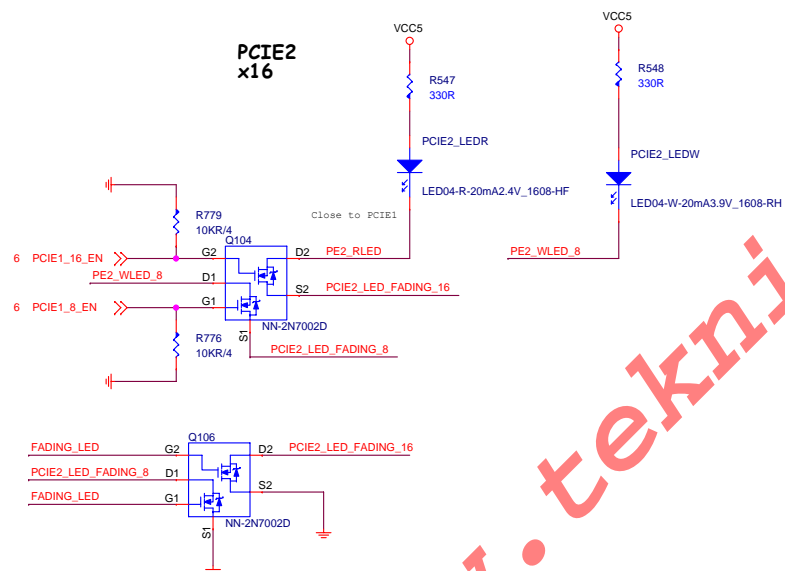


例：D0C-040S500-E07

LED 的 DIMM LED 设计



PCIE2
x16



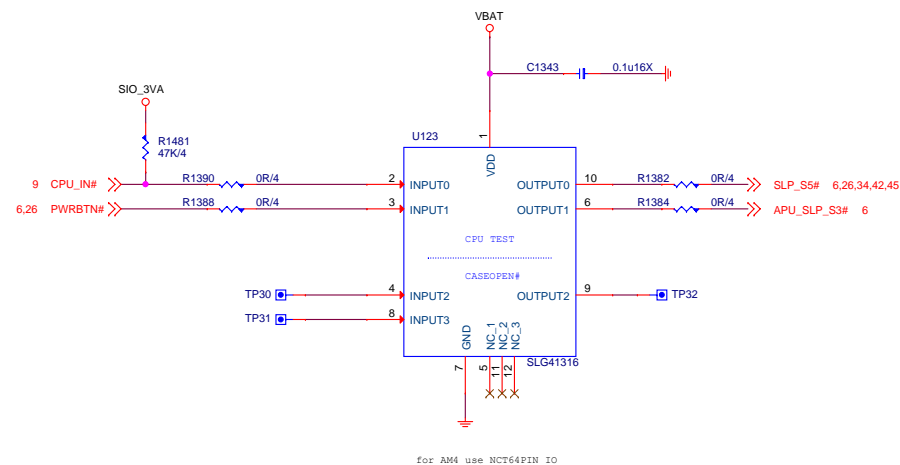
	x16	x8	x4
PCIE1	Red	X	X
PCIE4	X	White	X
PCIE6	X	X	White



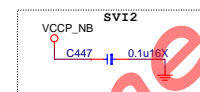
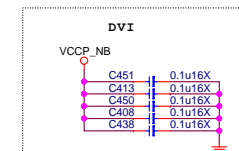
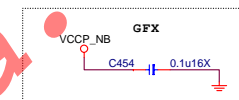
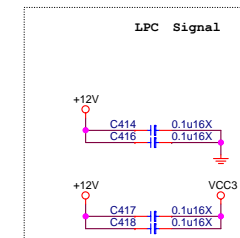
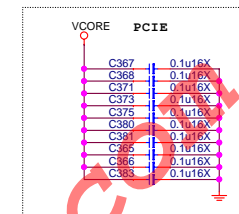
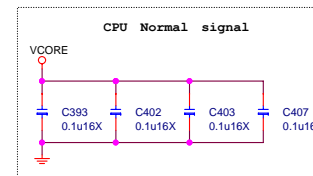
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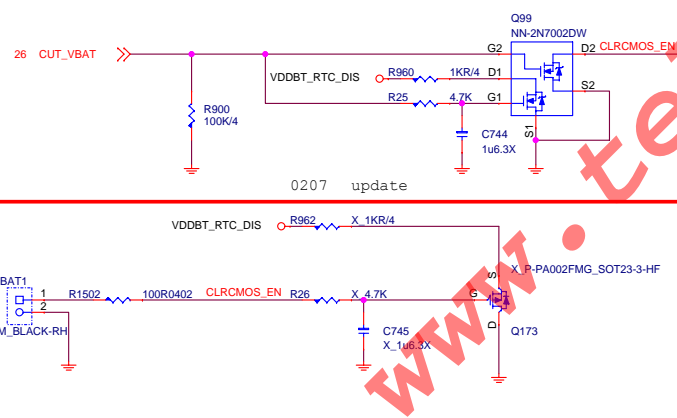
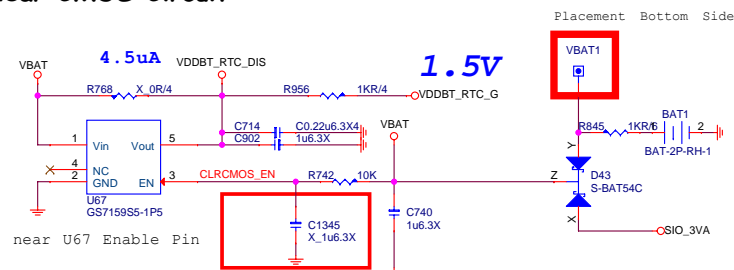
Size Custom	Document Description LED DIMM/PCIE	Rev 11
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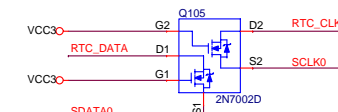
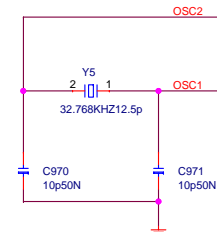
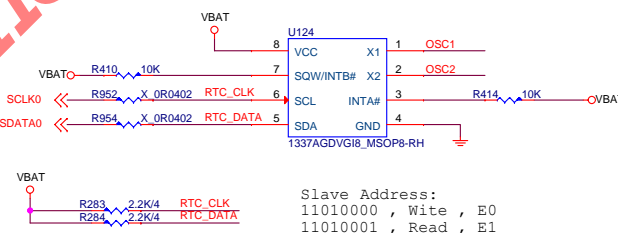
Moat Cap



RTC & Clear CMOS Circuit



0107 AM4 update

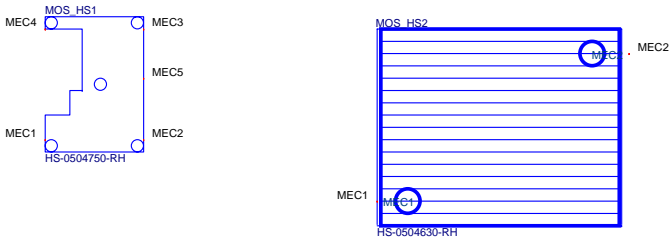


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Size	Document	Description	Rev
Custom		RTC Circuit/Moat Cap	11
Date:	Tuesday, March 07, 2017	Sheet	60 of 65

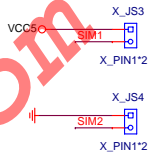
HEAT SINK



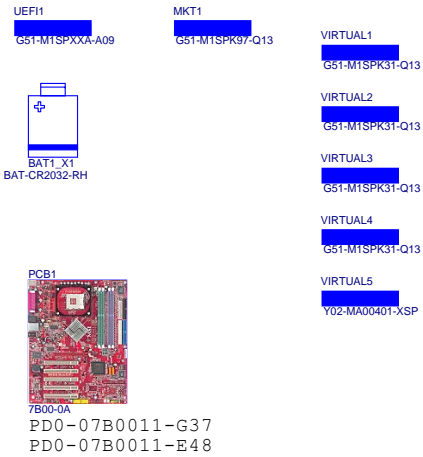
CPU Socket



Simulation

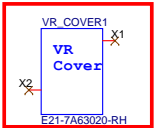


MANUAL PART



0901 Modify DDR_COVER1 PIN X1,X2,X3,X4,X5 Connect to GND for tiancai

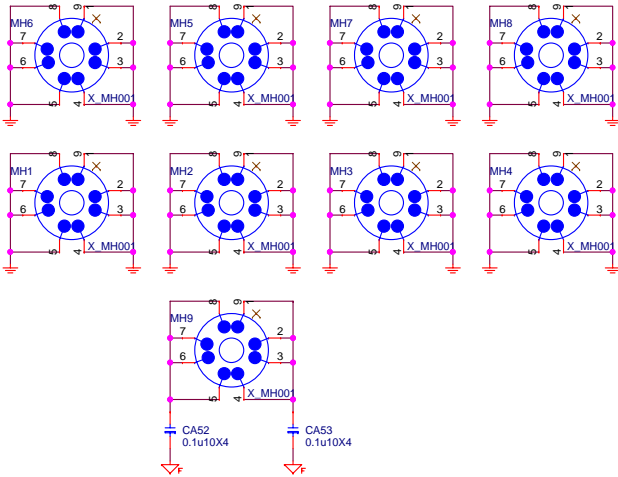
VR Cover



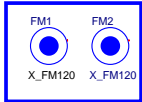
AUD_COVER1



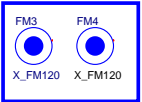
Optics Orientation Holes



5010



5020



FM5

FM6

FM7

FM8

X_FM120

X_FM120

X_FM120

X_FM120

OPT	Configure	BOM	Function
		XXXX	



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Custom	BOM Option		11
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